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A BUILT-IN SELF-TEST CIRCUITRY BASED ON RECONFIGURATION FOR ANALOG AND MIXED-SIGNAL IC

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Abstract. Application of built-in self-test circuitries allows to improve the testing quality and reliability of complex analog and mixed-signal IC. BIST-circuitry is integrated to original circuit for the purpose of test signal generation, measurement of output responses and decision-making about correctness of circuit under test functioning. The most part of BIST-circuitries for analog and mixed-signal IC uses generators of sine wave or multifrequency wave for test signal generation, but it is not applicable for majority of practical implementations because of crucial increasing the chip area required for in-circuit realization of generator. The built-in self test circuitry for analog and mixed-signal IC based on reconfiguring original circuit in oscillator, which does not need the generator of input test signals, has been proposed. The principles of functioning and main components of the solution have been considered. The correct and incorrect behaviour of analog subcircuit is reflected in digital way by logical 0 or 1. The proposed circuitry provides possibility for joint testing analog and digital subcircuits of mixed-signal IC. The experimental results for benchmark second-order active filter demonstrating high efficiency of proposed BIST-circuitry have been represented. The fault coverage obtained by application of proposed BIST-circuitry is not inferior to results of other authors for the same filter, but measuring and estimation of output responses are performed in-circuit.

Keywords: analog and mixed-signal integrated circuits, built-in self-test (BIST), reconfiguration, oscillator, design-for-testability (DFT).

1. Introduction

There are several reasons of high complexity of analog circuits testing, the main of which are tolerance range of internal components parameters, and consequently tolerance of output characteristics, continuous character of signal transformation, nonlinear dependence between output and input signals, etc. The additional complication deals with restricted access to internal nodes of a device in the case of integrated realization.

Many problems in testing could be overcome by using of structural solution of built-in self-test (*BIST*) realized in the framework of design-for-testability approach (*DFT*) [1]. BIST-solutions are placed in a chip together with designed devices for the purpose of test signal generation, measurement of output responses and decision-making about quality of circuit under test functioning. The BIST-circuitries are realized on early stages of IC design process. It provides optimal conditions for the next reliable testing of completely realized device. Such an approach is effective for both analog and mixed-signal IC.

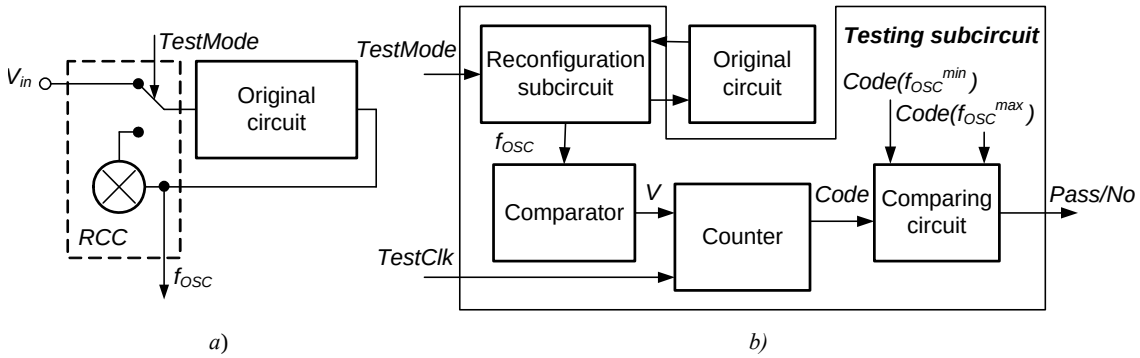
The most part of proposed BIST-solutions uses generators of sine wave or multifrequency wave represented by sum or sequence of sine waves for test signal generation [2, 3]. However, such a solution is not applicable for the majority of mixed-signal IC because of crucial increasing the chip area required for in-circuit realization of generator.

The common concept of approach to testing analog IC based on reconfiguration of original circuit in oscillator, which does not need the generator of input test signals, was proposed in [4]. This concept was called as Oscillation-BIST (*OBIST*). In papers of many authors who use this concept the main attention is paid to ways of transformation the original circuit to oscillator [5 – 8]. The topics of measurement the oscillating frequency and decision-making about functional correspondence of tested circuit were not studied completely.

The built-in self-test circuitry based on OBIST concept and oriented at the usage for analog and mixed-signal IC when analog subcircuit can be tested jointly with digital part is proposed in the paper. The solution takes into account tolerances on parameters of analog subcircuits' internal components. The main attention is paid to architecture of the testing subcurcuit, realization of the measurement circuit and the estimating oscillated frequency of a circuit under test.

2. Main concept

Testing based on circuit reconfiguration can be realized only in off-line mode because requires a transformation of original circuit in an oscillator. For that purpose, reconfiguration circuitry (*RCC*) activated by signal *TestMode* switches-off the source of input signal from the circuit and provides organization in the device global and/or local feedback (Figure 1, *a*). The periodical signal of arbitrary shape with frequency f_{OSC} is generated in the testing mode after finishing all transient processes at oscillator.



a) *b)*

Figure 1. Structural circuit of Oscillation-BIST: *a*) common case; *b*) proposed solution

Self-excitation frequency f_{OSC} is a controlled parameter of reconfigured circuit, measurement and analysis of which provide the decision-making about functionality of the original circuit [9].

In order to provide the completeness of test it is possible to use several internal nodes. However, in this case both the complexity of controlling the reconfiguration subcircuit and hardware expenses are increased. Direct measurement of analog signal frequency is long enough process which needs special measuring equipment and, as result, brings to a decreasing the economical efficiency of testing. The solution of in-circuit measuring and estimation of controlled frequency f_{OSC} based on OBIST concept is proposed (Figure 1, *b*). The digital code corresponding to measured self-excitation frequency is offered for using during testing instead of exact value of f_{OSC}. The comparator and digital counter are used for generation of such code. The comparator transforms the output signal of the oscillator in the sequence of rectangle pulses with period proportional to f_{OSC} and voltage level from 0 to V_{dd}.

The counter after finishing all transient processes in the circuit under test provides an enumeration of pulses quantity of clock signal *TestClk* during one period of signal *V*. The value of frequency for clock signal *TestClk* is selected as no less than $]\,60\,f_{OSC}\,[$ what provides the measurement error no more than 0.8 %.

The counter contains the control unit (Fig. 2) which provides initialization of register-counter and detection of rising edge of input pulse sequence after fixed time delay corresponding to finish all transient processes at oscillator. The control unit (*CU*) validates the start of an enumeration of clock signal *TestClk* pulses quantity. The CU stops counting after detection the rising edge of next pulse of input sequence. The calculated digital code is kept in register-counter, the length of which is calculated using the lower bound of confidence limit for frequency f_{OSC} of fault-free circuits taking into account the tolerance on circuit's components

$$n(REG) = \left\rceil \log_2\left(\frac{1}{T_{TestClk}\ f_{OSC}^{\min}}\right)\right\lceil + 1,$$

where $T_{TestClk}$ – the period of clock signal *TestClk*, $f_{OSC}^{\min}$ – the lower bound of confidence limits for frequency f_{OSC} deviation.

The presence of tolerances for parameters of internal components of fault-free circuit has influence on the value of self-excitation frequency. The Monte-Carlo method was used in order to estimate the confidence limit for frequency f_{OSC} of fault-free circuit taking into account internal component tolerance. The calculation of frequency f_{OSC_i} is performed for each iteration *i*. The parameters for internal components are assigned in casual way with specified mathematical expectation and standard deviation at each iteration step taking into account the tolerance for each type of elements. In order to get more exact confidence limit for frequency deviation it is recommended to use a distribution law and values of moments distinctive to integrated technology and technological line where IC will be realized. The digital codes are generated for all values f_{OSC_i}. The upper and lower limits of fault-free circuit range are defined with specified reliability. The digital code of CUT measured frequency is compared with the range limits. When digital code is placed outside the confidence limits, the original circuit is considered as faulty. The result of frequency comparison is represented as FALSE or TRUE. So, the correct or incorrect behaviour of analog circuit is reflected in digital way by logical 0 or 1. The resulting bit of the proposed testing subcircuit may be used together with boundary scan techniques or BIST-circuitries applied for testing the digital subcircuit of a mixed-signal circuit. Thus, the proposed solution provides a possibility for joint testing both analog and digital subcircuits of mixed-signal IC.

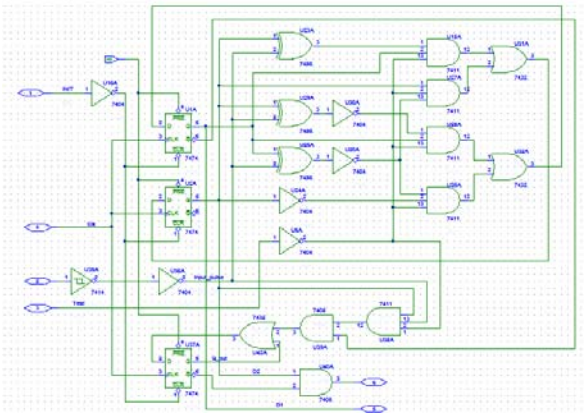


Figure 2. Circuit of counter control unit

3. Practical implementation

The proposed solution was considered on the typical benchmark circuit of second-order active filter (Figure 3). The tolerance on internal parameters was set up as ± 5 % for resistors and ± 10 % for capacitors. The nodes 1, 2 and 3 are circuit's outputs of HPF, BPF and LPF, respectively. The BPF output has been selected as a test node because signal measured in it possesses the higher value of sensitivity to deviation of internal components' parameters calculated for the self-excitation frequency. The sensitivity analysis was performed using *MATLAB* software.

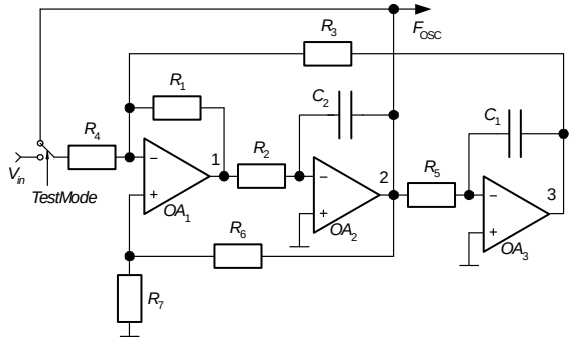


Figure 3. Second-order active filter

Simulation in time domain was performed using *PSpice* (*CADENCE*) CAD tools. In testing mode, the generated signal in node 2 of active filter with nominal values of internal parameters has shape shown

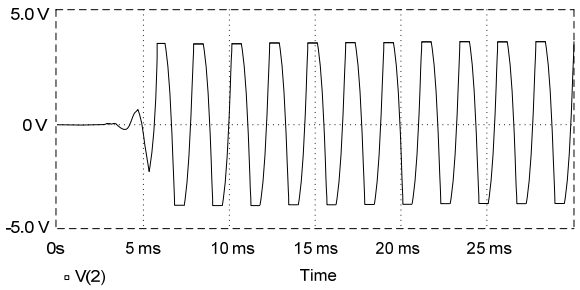


Figure 4. Output signal of active filter (BPF) in the testing mode

in Figure 4. The simulation provides an estimation of duration the transient processes in CUT equal to 6 ms. The measurement of self-excitation frequency f_{OSC} can be realized after 8 ms since the start of testing. The self-excitation frequency (f_{OSC} = 446 Hz) has been obtained at simulation of the filter with nominal parameters. The estimation of frequency deviation range taking into account tolerances of internal components was done by Monte-Carlo method realized using *PSpice*, where the value of parameter for each internal component p_i on each iteration step is calculated as

$$p_i = p_{nom\_i}\left(1+\Delta_i\xi_i\right),$$

where p_{nom_i} – nominal value of the *i*-th component in the netlist; Δ_i – relative deviation of parameters p_i; ξ_i – centered casual value distributed in range (–1, +1) by normal law with mathematical expectation equal to 0 and standard deviation $\sigma = 0.25$.

The statistics of realized trials by Monte-Carlo method with the number of iterations 5 000 is shown in Figure 5. The quantity of iterations has been selected according to minimum quantity of steps for specified reliability and some limitations of CAD tools. According to the obtained results the upper and lower confidence limits for frequency of faulty-free circuit with reliability $\gamma = 0.997$ are equal to 380 Hz and 520 Hz respectively, and with reliability $\gamma = 0.9$ are equal to 413 Hz and 486 Hz respectively.

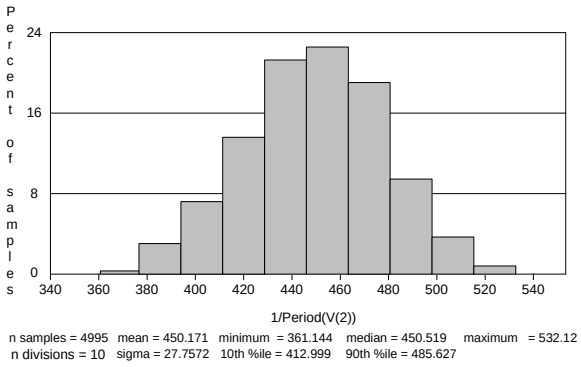


Figure 5. Statistics of Monte-Carlo iterations for frequency confidential range

The effectiveness of the proposed solutions was estimated for single faults. Both catastrophic and parametric faults were considered. Catastrophic faults deal with short or open effects in the circuit of the filter. Parametric faults are stipulated by deviation of component parameters outside the tolerance range. During experiment the parametric faults for resistors and capacitors were appointed as parameter deviation on value ± 20 % and ± 50 % from the nominals. The simulation of the proposed BIST circuitry for the second-order active filter provided the detection 100 % of catastrophic faults. The following results were obtained for parametric faults: detection of 53.6 % at using confidential limit with reliability $\gamma = 0.997$ and 78.6 % at using confidential limit with

reliability $\gamma = 0.9$ (Table 1). Analysis of the obtained results demonstrates high efficiency of the proposed solution at testing the second-order active filter.

The fault coverage obtained by the proposed solution is high and not inferior to results of other authors for the same typical benchmark active filter, but measuring and estimation of output responses are performed in-circuit.

Table 1. Results of fault simulation

Type of fault									
Catastrophic			**Parametric**						
Type	f_{OSC}	**Detected**	**Type**	f_{OSC}	**Detected**		**Type**	f_{OSC}	**Detected**	
					$\gamma = 0.9$	$\gamma = 0.997$			$\gamma = 0.9$	$\gamma = 0.997$
C_1_short	const	+	C_1 +20%	404	–	–	C_1 +50%	360	+	+
C_1_open	1450	+	C_1 –20%	505	+	–	C_1 –50%	649	+	+
C_2_short	const	+	C_2 +20%	243	–	–	C_2 +50%	373	+	+
C_2_open	12500	+	C_2 –20%	202	+	–	C_2 –50%	621	+	+
R_1_short	const	+	R_1 +20%	526	+	+	R_1 +50%	592	+	+
R_1_open	const	+	R_1 –20%	173	+	+	R_1 –50%	const	+	+
R_2_short	const	+	R_2 +20%	469	–	–	R_2 +50%	492	+	–
R_2_open	578	+	R_2 –20%	420	+	–	R_2 –50%	361	+	+
R_3_short	1429	+	R_3 +20%	404	–	–	R_3 +50%	360	–	–
R_3_open	const	+	R_3 –20%	507	+	–	R_3 –50%	645	+	+
R_4_short	11111	+	R_4 +20%	413	–	–	R_4 +50%	371	+	–
R_4_open	const	+	R_4 –20%	495	+	–	R_4 –50%	621	+	+
R_5_short	const	+	R_5 +20%	294	+	+	R_5 +50%	const	+	+
R_5_open	const	+	R_5 –20%	568	+	+	R_5 –50%	709	+	+

4. Conclusion

The built-in self-test circuitry based on reconfiguration to oscillator has been proposed for analog and mixed-signal circuits. The technique for measurement and estimation of self-excitation frequency has been described. The testing subcircuit contains reconfiguration circuitry, comparator, counter and comparing circuit and needs small area of chip for implementation.

The proposed solution can be used for testing both analog and mixed-signal circuits due to compatibility with methods of signature analysis and boundary-scan of digital subcircuits. The experimental results obtained for benchmark circuit shown high efficiency of the proposed solution, which provides 100 % coverage of catastrophic faults and $53.6\,\%\big|_{\gamma=0.997}$ and $78.6\,\%\big|_{\gamma=0.9}$ of parametric faults.

The future development of idea deals with preparing a subsystem of CAD tools for design-for-testability of analog and mixed-signal circuits, providing complex support of design stages for OBIST including selection of circuit for reconfiguring original device to oscillator, automated adjustment of in-circuit testing circuitry for any specific final realization, and also selection of ways to integration with digital BIST circuits.

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