

ITC 2/53 Information Technology and Control Vol. 53 / No. 2 / 2024 pp. 509-521 DOI 10.5755/j01.itc.53.2.35652	An Improved YOLOv5x-Based Algorithm for IC Pin Welding Defects Detection	
	Received 2023/11/19	Accepted after revision 2024/04/29
	HOW TO CITE: Wang, X., Li, M., Hu, X., Guo, B. (2024). An Improved YOLOv5x-Based Algorithm for IC Pin Welding Defects Detection. <i>Information Technology and Control</i> , 53(2), 509-521. https://doi.org/10.5755/j01.itc.53.2.35652	

An Improved YOLOv5x-Based Algorithm for IC Pin Welding Defects Detection

Xueying Wang, Mengyun Li, Xiaofeng Hu, Bin Guo

School of Measurement and Testing Engineering, China Jiliang University, Hangzhou, Zhejiang 310018, China; e-mails: xueyingwang@cjlu.edu.cn; 1090533157@qq.com; 12b0202094@cjlu.edu.cn; guobin905@cjlu.edu.cn

Corresponding author: xueyingwang@cjlu.edu.cn

This study suggests an integrated circuit (IC) pin welding defect detection algorithm based on improved YOLOv5x to address the issues of low detection accuracy caused by small target size and dense pin arrangement in IC pin welding defects identification. The ability of the network to extract features is improved by effective fusing of features with various receptive fields through the inclusion of the D-SPP module to merge different channel information. The introduction of the mask self-attention mechanism module increases the network's capacity to recognize global feature correlations and raises the algorithm's detection precision. In order to speed up the model's convergence and tackle the issue of sample imbalance in BBox regression, the Focal-EIoU loss function is applied. The detection accuracy and speed are increased by using the k-means++ clustering algorithm to create nine clustering centers to figure out the size of the prior box. According to the results of the experiment, the new method achieves average precisions for short-circuit, missing pin, pin-cocked, and little tin faults in IC pin welding of 96.7%, 94.5%, 95.6%, and 93.3%, respectively. The mean average precision increases to 95.0% at a threshold of 0.5, which is 13.3% and 8.9% greater than YOLOv3 and YOLOv5x, respectively. A reference value for IC pin welding defect identification is provided by the improved algorithm, which has a detection time of 0.142 seconds per image. This meets the speed requirements of IC quality inspection.

KEYWORDS: IC pin welding defect detection, YOLOv5x, D-SPP module, Mask self-attention mechanism, Focal-EIoU, k-means++.

1. Introduction

With the rapid development of information technology, the integration level of electronic products is increasing, and they are gradually becoming smaller,

more intelligent, and more integrated. IC has become increasingly important in the information industry and are widely used in the fields of electronics, semi-

conductors, and artificial intelligence [23]. After the IC chip and other electronic components go through processes such as silk screen printing and surface mount technology (SMT), they are welded on the printed circuit board (PCB) and ultimately used to implement corresponding functions in electronic products [30]. Whether various electronic products can operate normally and the length of their service life are closely related to the quality of the PCB. The quality of the PCB depends on the welding quality of its electronic components. If PCBs with welding problems enter the market for assembly and production, they may cause equipment damage during use, which could result in significant economic losses and even endanger personal safety in severe cases [28]. Therefore, it is necessary to perform fast and accurate detection of PCB defects in the production process, among which IC pin welding defect detection is one of the most important detections in PCB defect detection. IC pin welding defect detection can effectively prevent defective circuit boards from entering subsequent processes and minimize losses as much as possible.

2. Related Works

Traditional PCB defect detection methods include visual inspection, online testing, and functional testing [22]. Among them, visual inspection relies on human eyesight to directly observe the circuit board through equipment such as magnifying glasses. Its main advantages are low cost and no need for fixtures or other equipment. However, its disadvantages are that it is easily affected by subjective factors such as the work experience and emotions of the personnel, leading to lower accuracy and efficiency in defect detection. The main method of online testing is flying probe testing, which has the advantages of flexibility and fast testing. However, it belongs to contact measurement and may cause secondary damage to the circuit board to a certain extent. Functional testing is based on the principle of automated testing and uses various testing equipment to test specific boards or units. Its disadvantages are slow testing speed and lack of support for parameter measurement.

Machine vision is a non-contact and non-destructive automatic inspection technology [24], which has developed rapidly in recent years and has been widely applied in industrial quality inspection. The applica-

tion of machine vision for PCB defect detection has also received much attention. Keenan et al. [9] developed a non-invasive technique for photographing the component circuits of ICs and used infrared laser beam detection technology to inspect flaws in integrated circuits on PCBs. Yamada et al. [29] used high-sensitivity micro eddy current probes along with image processing technologies. By using differential and filtering operations between standard images and test images of PCBs, Ibrahim et al. [6] successfully reduced the noise produced during image preprocessing, minimizing errors or uneven binarization. In order to fully detect PCB defects, Kumar et al. [10] suggested picture enhancing techniques as color plane extraction and LUT transformation, as well as a standard data creation approach. In order to efficiently identify flaws in bare PCBs such as etching, short circuits, and open circuits, Kaur et al. [8] proposed applying image differential operations. Gaidhane et al. [3] used a similarity measurement technique that allowed for the direct quantification of similarity between scene photos of PCB surfaces and reference images without the need for image feature computations. In summary, methods based on traditional image processing and machine vision have some progress, with basic steps such as feature extraction and template matching. However, for different PCBs, re-modeling is required, which has the shortcomings of being time-consuming and cumbersome.

In recent years, with the successful application of deep learning models in fields such as face recognition, defect detection and object tracking [27, 31, 15], deep learning-based PCB defect detection has also developed rapidly. Park et al. [17] developed the Mars-Net construction, which improves the Dilated Residual Network (DRN) to increase feature map resolution. Additionally, they created Horizontal Vertical Pooling (HVP) to improve pooling efficiency by obtaining positioning data from the feature maps. In order to improve PCB defect detection performance, Ding et al. [2] created a Tiny Defect Detection Network (TDD-Net) based on Faster R-CNN. This network improves the connections between feature maps at different levels. A cascaded CNN network was utilized by Cai et al. [1] to identify SMT welding junctions. Two other CNN networks received the input image and the adaptive image learning results from one CNN network. This approach eliminates the requirement to extract low-level features by simply completing the detection operation. Ran et al. [18] proposed a PCB defect detec-

tion and recognition algorithm based on SSD, which customizes different scale bounding boxes using multi-scale feature mapping, predicts classification results and boundary box information using small convolution kernels, and optimizes the detection results using NMS algorithm. The Edge and Multi-scale Reverse Attention Network (EMRA-Net), created by Lin et al. [11], incorporates a new Pyramid Edge Module and a Multi-scale Fusion (MSF) module in the feature extraction procedure. These modules are used to obtain features with different resolutions and sizes. A CNN-based two-stage object detection framework was developed by Luo et al. [16]. They used a Locally Non-Local (LNL) module to improve defect classification accuracy and a Multi-Hierarchical Aggregation (MHA) module to improve the localization accuracy of non-prominent faults. While the above networks enhance the accuracy of defect detection to a certain extent, they are not without limitations.

Particularly, in cases where the dataset is large, the excessive computation can significantly impact both the learning process of the model and the detection speed. Consequently, they fail to meet the real-time detection requirements.

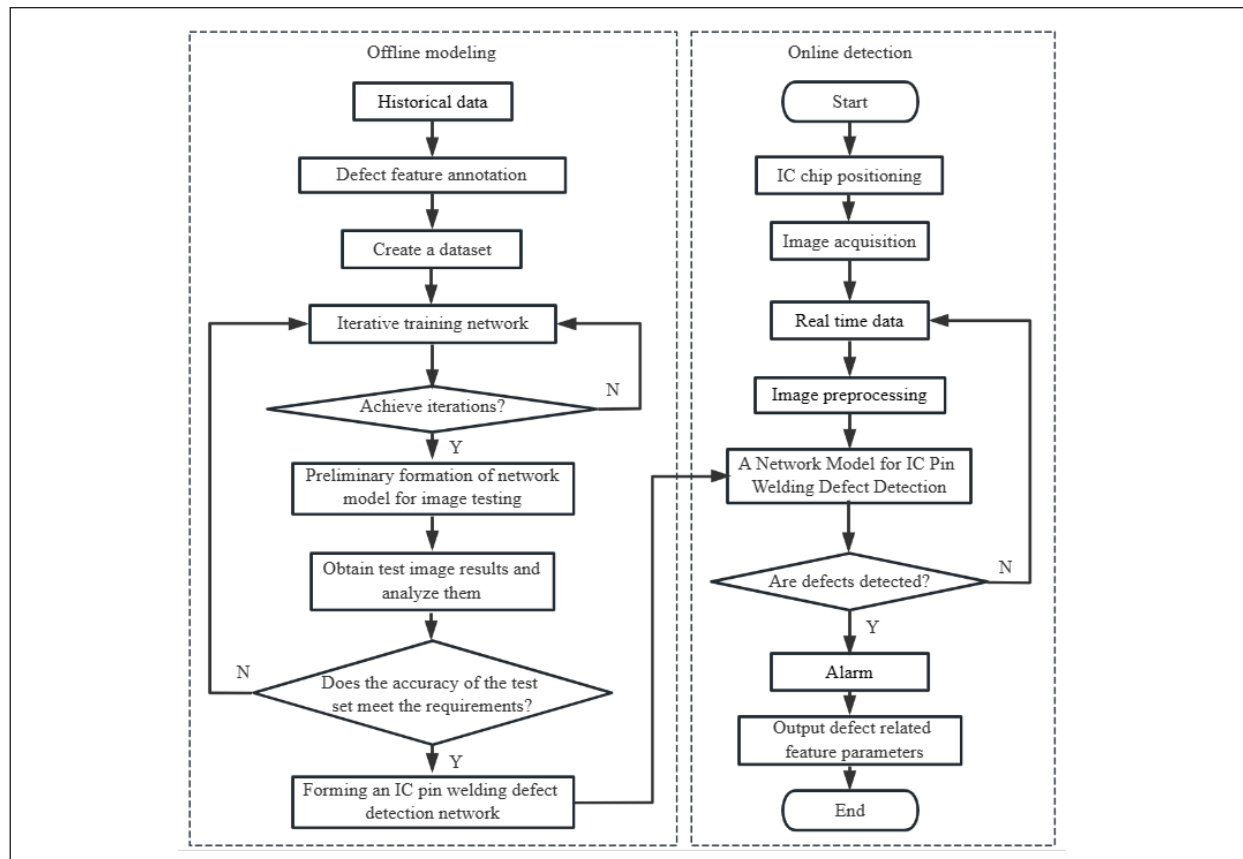
3. Our Approach

3.1. Testing Process

In order to solve the difficulty in detection of small and dense IC pins, this paper proposes an improved YOLOv5x algorithm to detect defects in IC pin welding. The detection process diagram is given in Figure 1, and the specific procedure of model establishment can be divided into the following four steps:

- a Firstly, annotate the collected IC pin welding defect images and create a dataset in Pascal VOC format.

Figure 1
Detection flow chart



- b Secondly, partition the dataset into a training set, a validation set, and a test set in a 6:2:2 ratio.
- c Next, input the training set and validation set into the improved YOLOv5x network for iterative optimization of network parameters to accelerate network convergence.
- d Finally, after completing the model training, evaluate the network's ability to detect new defect images using the test set. If the model's performance meets the requirements, apply the model to the online detection system; otherwise, optimize the network and continue training.

3.2. Network Model Algorithm

Deep learning-based object detection algorithms can be broadly categorized into two types: two-stage detection algorithms and one-stage detection algorithms. On the one hand, two-stage object detection algorithms divide the detection task into two stages. First, they identify candidate regions where objects may be present and make preliminary judgments about whether they contain objects. Then, they classify and regress these candidate regions to refine their positions and ultimately output the object's category. Representative algorithms in this category include R-CNN [4], Fast R-CNN [5], and Faster R-CNN [21]. On the other hand, one-stage object detection algorithms do not have a separate stage for generating

candidate regions. Instead, they directly output the probability of object categories along with the corresponding position coordinates. Representative algorithms in this category include YOLO [19], YOLOv3 [20], SSD [14], and others.

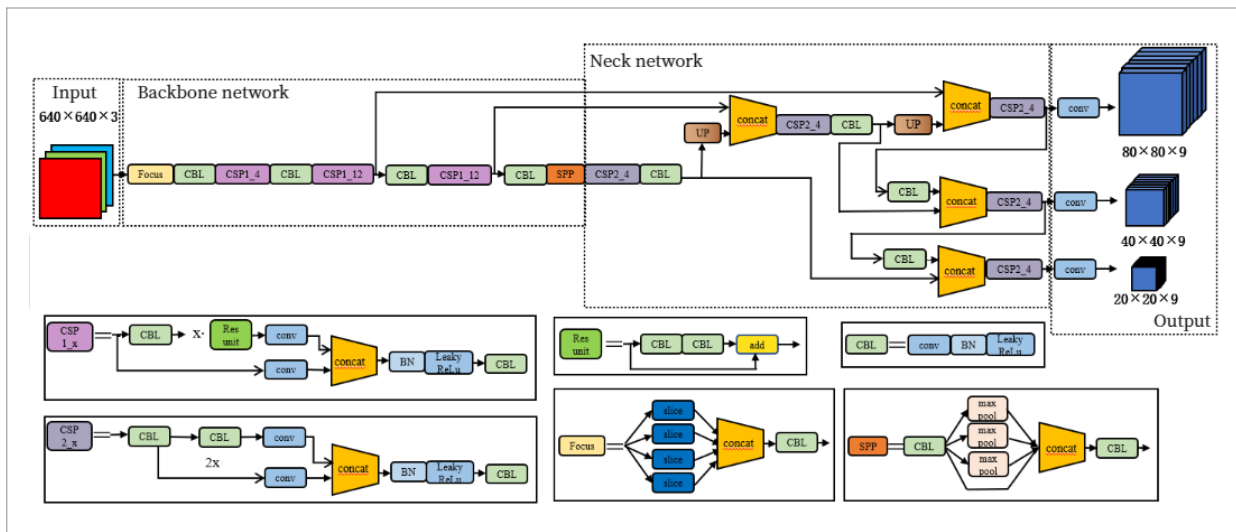
In 2020, Jocher et al. [7] introduced the YOLOv5 algorithm. YOLOv5 comprises five different models, namely YOLOv5n, YOLOv5s, YOLOv5m, YOLOv5l, and YOLOv5x. These five models share a common internal structure but differ in their depth and width factors. Consequently, the models vary in size, parameter count, network depth, detection accuracy, and detection speed. Notably, YOLOv5x exhibits exceptional detection accuracy. Therefore, this paper selects the YOLOv5x model for the design of the IC pin welding defect detection algorithm.

3.2.1. YOLOv5x Network Model

The network structure of IC pin welding defect detection based on YOLOv5x is shown in Figure 2. The backbone network is the CSPDarknet53 network [26], the neck network is a combination of Feature Pyramid Networks (FPN) [12] and Path Aggregation Network (PAN) [13], and the detection head has outputs in three different scales. The IC pin welding defect detection network based on YOLOv5x includes two types of CSP structures: CSP1_x and CSP2_x. The CSP1_x, Focus, and SPP structures are used to improve the backbone network, while the CSP2_x, FPN,

Figure 2

The network structure diagram of IC pin welding defect detection based on YOLOv5x



and PAN are combined to form the neck network, which strengthens the fusion of features at different scales and enhances the network’s ability to extract features of IC pin welding defects.

3.2.2. Improved YOLOv5x Network Model

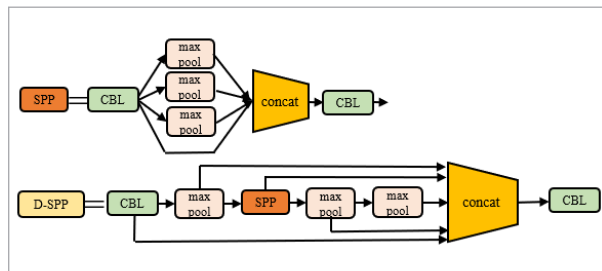
The algorithm presented in this paper is an enhancement built upon the foundation of the YOLOv5x algorithm. The following sections provide an introduction to the modifications made in three aspects: D-SPP, Masked Self-Attention Mechanism, and Loss Function.

1 D-SPP Module

The YOLOv5x algorithm uses the SPP module in the backbone network to obtain information at different receptive field sizes. However, the SPP module cannot fully integrate local and global information, which may result in information loss. This paper proposes the D-SPP module, as shown in Figure 3. The structure adopts a method similar to spatial attention to embed SPP into SPPF to generate adaptive weights for features at different scales. By combining information from different channels, features from different receptive fields can be efficiently fused, enhancing feature representation capacity.

The D-SPP module generates adaptive spatial weights for features with different receptive fields through a combination of convolutional and pooling operations. Initially, it employs pooling branches with fixed scales and then utilizes the SPP module to extract information, embedding spatial details. By weighting and fusing contextual features, it generates new features enriched with multiscale contextual information. These newly generated feature maps, obtained through two successive max-pooling operations, are subsequently fused with the previously obtained feature maps.

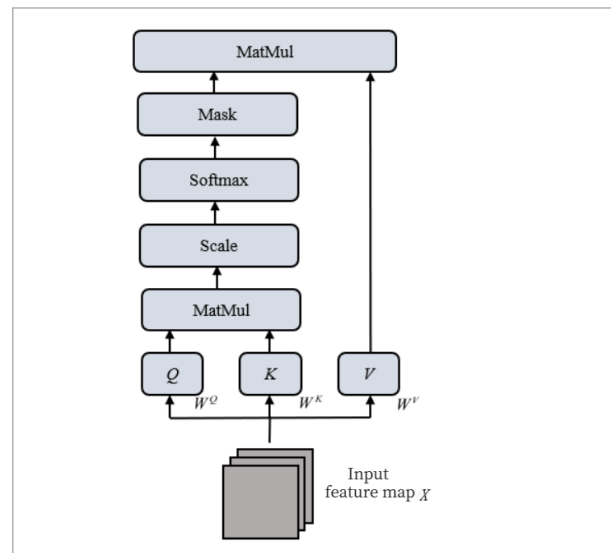
Figure 3
D-SPP structure diagram



2 Masked Self-Attention Mechanism

This paper introduces a Masked Self-Attention Mechanism module [25] to enhance the network’s ability to capture global feature relationships. The module is embedded after the output of the effective feature layer and before the input of the prediction layer in the neck network. The Masked Self-Attention Mechanism operates on feature maps of three sizes: large, medium, and small, to detect IC pin welding defects at multiple scales, thereby improving detection accuracy of the algorithm. The structure of Masked Self-Attention Mechanism module is shown in Figure 4.

Figure 4
Structure diagram of Masked Self-Attention Mechanism



In Figure 4, the input feature map X is multiplied by convolution kernels W^Q , W^K and W^V to generate query vector matrix Q , key vector matrix K and value vector matrix V , respectively. By performing inner product operations on query vector matrix Q and key vector matrix K through scaled dot-product, attention scores are obtained through Softmax activation function normalization. The attention scores are then subject to mask calculation, and finally multiplied by value vector matrix V to obtain the output of self-attention. The output of the Masked Self-Attention module is shown in Equation (1).

$$Z = \text{Softmax} \left(\frac{QK^T}{\sqrt{d_q}} \right)_{\text{mask}} V. \tag{1}$$

3 Loss Function

The loss function of the improved YOLOv5x algorithm consists of confidence loss, classification loss and boundary box regression loss. The confidence loss and classification loss are calculated using binary cross-entropy loss function, while the boundary box regression loss is calculated using Focal-EIoU. In Focal-EIoU Loss, the width and height losses directly minimize the difference between the widths and heights of target box and anchor box, which speeds up convergence and solves the vague definition problem of CIoU aspect ratio. Furthermore, Focal Loss is added to address the sample imbalance problem in BBox regression. The formulas for calculating Focal-EIoU Loss are shown in Equations (2)-(3). The complete loss function is shown in Equation (4).

$$L_{EIoU} = L_{IoU} + L_{dis} + L_{asp} = 1 - IoU + \frac{\rho^2(b, b^{gt})}{c^2} + \frac{\rho^2(w, w^{gt})}{C_w^2} + \frac{\rho^2(h, h^{gt})}{C_h^2} \quad (2)$$

$$L_{Focal-EIoU} = IoU^\gamma L_{EIoU} \quad (3)$$

$$Loss = L_{Focal-EIoU} + \sum_{i=0}^{S \times S} \sum_{j=0}^B L_{ij}^{obj} [\hat{C}_i \log(C_i) + (1 - \hat{C}_i) \log(1 - C_i)] - \sum_{i=0}^{S \times S} \sum_{j=0}^B L_{ij}^{noobj} [\hat{C}_i \log(C_i) + (1 - \hat{C}_i) \log(1 - C_i)] + \sum_{i=0}^{S \times S} \sum_{j=0}^B L_{ij}^{obj} \sum_{cclasses} [\hat{p}_i(c) \log(p_i(c)) + (1 - \hat{p}_i(c)) \log(1 - p_i(c))] \quad (4)$$

In Equation (4), L_{ij}^{obj} and L_{ij}^{noobj} represent the probabilities of the j th anchor box in the i th grid containing and not containing defects, respectively. The value is 1 when the box contains defects, and 0 otherwise. \hat{C}_i represents the confidence level of the j th predicted box in the i th grid, while C_i represents the confidence level of the truth box. \hat{p}_i represents the probability value of the predicted box for its class, and p_i represents the probability value of the truth box for its class.

3.3. Evaluation Indicators

In the task of detecting defects in IC pin welding, the performance of the algorithm is mainly evaluated based on its detection accuracy and speed. The detection accuracy mainly includes Average Precision (AP)

and Mean Average Precision (mAP). Detection speed is generally measured in Frames Per Second (FPS).

1 AP is a metric used to assess the detection accuracy of individual defect categories within the IC pin welding defect dataset. AP is determined by the area under the Precision-Recall curve, with both precision and recall calculated from the confusion matrix. A higher AP value indicates a better detection performance for a particular category. The calculation method for AP is as follows:

$$AP = \int_0^1 P(r) dr, \quad r \in (0, 1) \quad (5)$$

$P(r)$ represents the function of the Precision-Recall (PR) curve.

2 mAP serves as a metric for assessing the detection accuracy across all defect categories within the IC pin welding defect dataset. mAP is calculated as the average of the AP values for each individual defect category. The calculation method for mAP is as follows:

$$mAP = \frac{1}{M} \sum_{i=1}^M AP_i. \quad (6)$$

M represents the number of defect categories, and in this study, we have focused on four distinct defect categories; therefore, $M=4$. Here, AP_i denotes the Average Precision for each individual defect class.

3 FPS represents the ratio between the total number of test samples and the time taken to perform detection on these test samples. The calculation formula is as follows:

$$FPS = \frac{N}{T}. \quad (7)$$

N represents the total number of test samples, and T represents the time expended for the detection process on these test samples.

4. Experiment Preparation

4.1. Image Acquisition

The experimental data in this paper was collected by the constructed image acquisition hardware platform. The computer issued the acquisition instruction, and

the motion controller controlled the PCB to move on the track and stop at the specified position. Then the light source was turned on, and the camera captured the image of the IC, which was then stored in the computer. A total of 1000 images were collected.

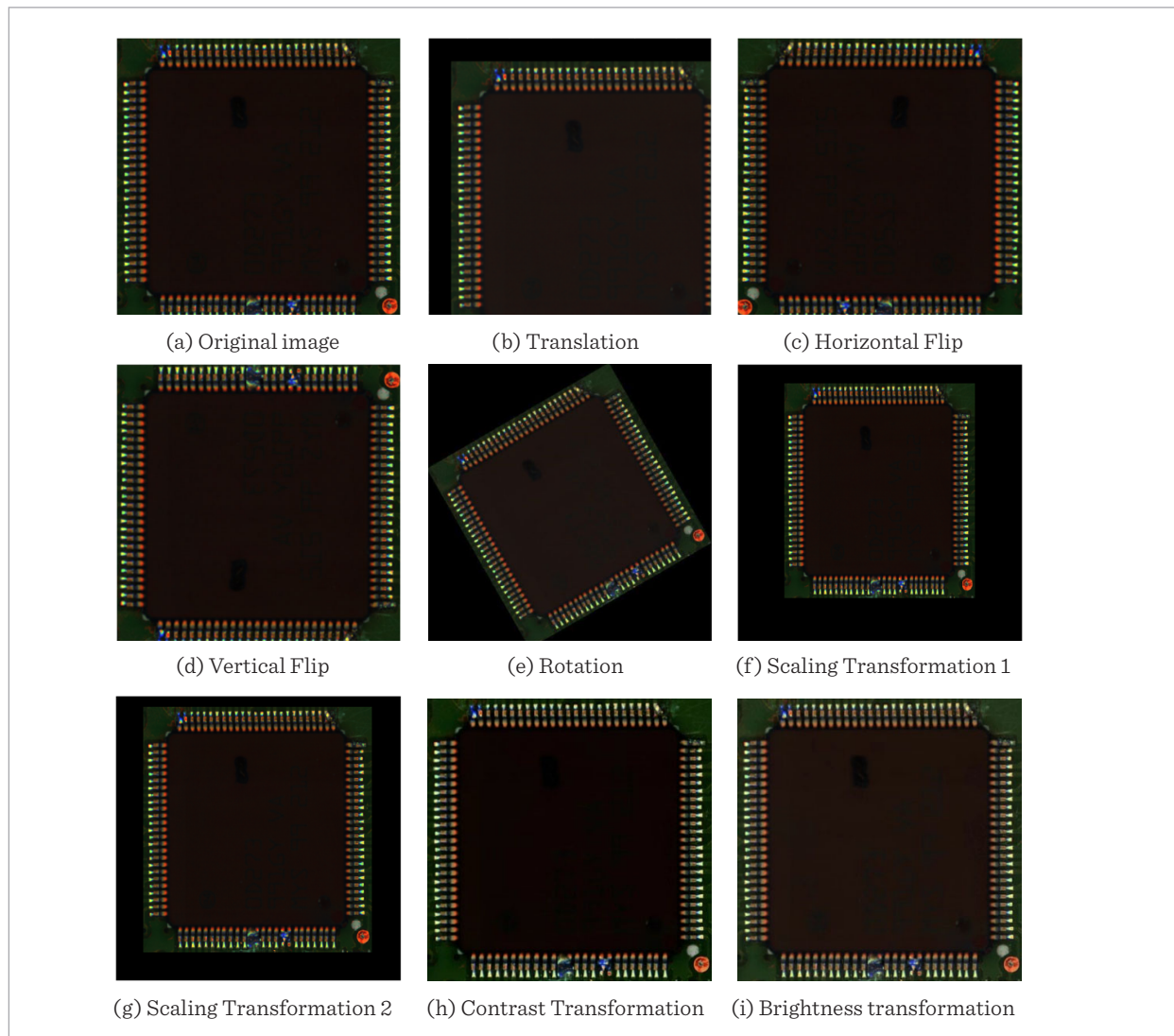
4.2. Data Enhancement

When the number of training samples is limited, the use of deep learning algorithms can often lead to overfitting, making it challenging to train robust models. Data augmentation is a commonly employed technique that mitigates overfitting and facilitates

the training of models with strong generalization capabilities, thereby enhancing defect recognition. Consequently, in this paper, seven data augmentation methods were used to expand the IC data samples, in order to enhance the richness of the data. The data augmentation methods are as follows: translation, horizontal flip, vertical flip, rotation, scaling transformation, contrast transformation, and brightness transformation. After data augmentation, a total of 10,000 images were obtained, and all the images were resized to 640×640 . Data augmentation examples are illustrated in Figure 5, as shown below.

Figure 5

Sample examples of data augmentation for IC pin welding defect images



4.3. Dataset Production

In order to make the collected image data more standard during model training and testing, the image data after data augmentation were made into a Pascal VOC format dataset. There are four types of IC pin welding defects obtained from the captured images, namely short circuit, missing pin, pin cocked, and little tin. LabelImg was selected to label the defects, and for each labeled image, a corresponding XML-format annotation file was generated. This file contains information such as the name and size of the image, the name of the defect, and the position information of the defect annotation box. The ratio of training set, validation set, and test set is 6:2:2.

5. Experiment and Analysis

5.1. Experimental Environment

The computational platform utilized for this study exhibits the following specifications: The CPU is Intel(R) Core(TM) i7-7700@3.60GHz; the GPU is NVIDIA GeForce GTX 1070; the system is equipped with 16 GB of RAM; the operating system employed is Windows 10. In terms of software components, the deep learning framework employed is PyTorch 1.8.0 (with torchvision 1.9.0), CUDA version 10.2, CUDNN version 7.6, and the programming language utilized is Python 3.7.

5.2. Configure Training Parameters

The dataset consists of 10,000 images, divided into 6,000 images for the training set, 2,000 images for the validation set, and 2,000 images for the test set. The combined size of the training and validation sets is 8,000 images. With a batch size of 20, this results in 400 batches and the input image size is 640×640. The initial learning rate is set to 0.00125, and the momentum parameter is set to 0.9. The entire training process is divided into 100 epochs, resulting in a total of 40,000 iterations.

YOLOv5x predicts defects using three feature maps of different scales, and each feature map contains three prediction values. Therefore, there are nine anchor parameters. The size and aspect ratios of the targets in different datasets vary. To more accurately identify the defects in the dataset created in this paper, an improved algorithm uses the k-means++ clustering

algorithm to cluster all defect box sizes, resulting in nine cluster centers: (19,60), (18,76), (72,21), (59,30), (56,38), (38,58), (49,84), (52,85), and (85,60).

5.3. Experimental Results and Analysis

To verify the performance of the improved network, under the same experimental conditions, the same IC pin welding defect dataset was applied to YOLOv3, YOLOv5x, and the improved network for 100 epochs, then the comparison of the loss value curves is shown in Figure 6.

Figure 6

Variation curve of training loss value of 3 models

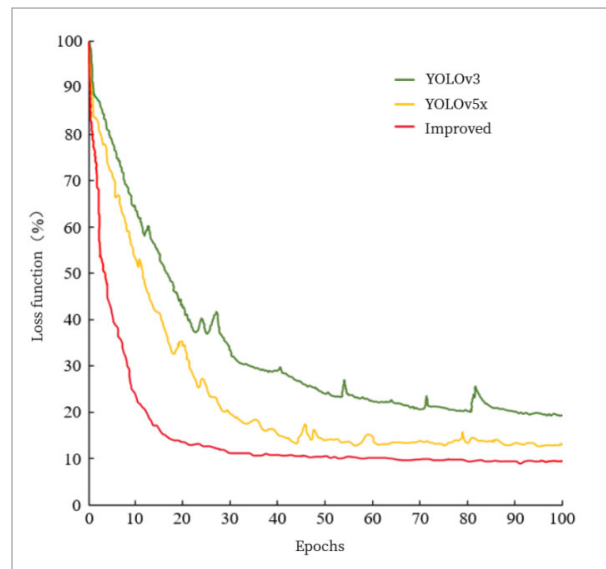


Figure 6 shows that with the increase of training epochs, the loss function curves of the three networks generally show a decreasing trend. The loss value curve of the YOLOv3 algorithm has a large oscillation amplitude and the slowest decrease rate. The loss value curve of the YOLOv5x algorithm has oscillation, but the decrease rate is faster than YOLOv3. The improved algorithm has the fastest decrease rate, and converges after about 30 rounds of training. After 100 epochs of iterative training, the loss value of the YOLOv3 algorithm is around 0.2, the loss value of the YOLOv5x algorithm converges to 0.14, and the loss value of the improved algorithm converges to 0.1. Compared with the other two algorithms, the improved algorithm has the smallest loss convergence

value. In conclusion, the loss curve of the improved algorithm has the smallest convergence value and tends to be stable, indicating that its training results are better than the other two algorithms.

During training, the validation set was used to verify the model performance every round of training. The comparison of the mean average precision (mAP) curve is shown in Figure 7.

Figure 7
The comparison of the mAP curves of 3 models

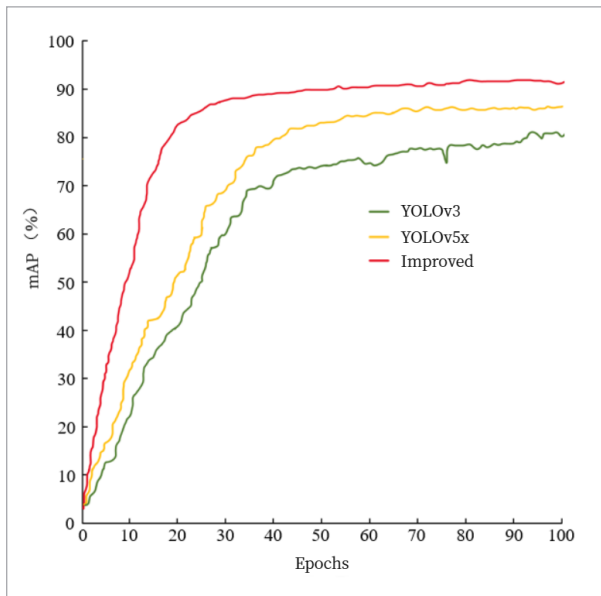


Figure 7 shows that with the increase of training epochs, the mAP curves of the three models generally show an upward trend. The mAP curve of YOLOv3 algorithm fluctuates and has the slowest increase rate. After 100 rounds of training, it is about 80%. The mAP curve of the YOLOv5x algorithm has a faster increase rate than YOLOv3, and after 80 rounds of training, the model's mAP stabilizes at around 86%. The mAP curve of the improved algorithm has the fastest convergence speed. After 50 rounds of training, the mAP stabilizes at around 90%.

A detailed comparison of the detection performance of the three models is provided in Table 1. It is notable that the YOLOv3 model exhibits a significant decrease in AP of 19.4% for short circuit and little tin defect, indicating a substantial drop in model performance as defect complexity increases. In contrast, the YOLOv5x model demonstrates a 12.3% decrease in AP for short circuit and little tin defect, suggesting an enhanced capability to recognize complex defects. The improved algorithm exhibits a maximum AP difference of 3.4% across the four defect categories, indicating a more balanced average detection accuracy for each defect type and a significant overall improvement in model performance. Under a threshold of 0.5, the mAP of the improved model reaches 95.0%, representing an increase of 13.3% and 8.9% when compared to YOLOv3 and YOLOv5x, respectively. Regarding detection speed, the improved model outperforms the other two models, offering faster detection capabilities.

Table 1
Comparison of detection performance of three models

Algorithm	AP (%)				mAP@0.5 (%)	detection speed (s/piece)	FPS (piece/s)
	short_circuit	missing_pin	pin_cocked	little_tin			
YOLOv3	89.5	82.7	84.4	70.1	81.7	0.257	4
YOLOv5x	90.6	86.9	88.7	78.3	86.1	0.208	5
Improved	96.7	94.5	95.6	93.3	95.0	0.142	7

To provide a more intuitive visualization of the performance of the three models in IC pin welding defect detection, each of the three models was employed to detect defects in two IC pin welding images. The results are illustrated in Figures 8-10.

The detection results are summarized and presented in Tables 2-3. It is evident from the results that the YOLOv3 algorithm missed one missing pin in the left image and incorrectly identified one little tin. While in the right image, it missed one pin cocked and false-

Figure 8

Visualization of detection results of YOLOv3 algorithm

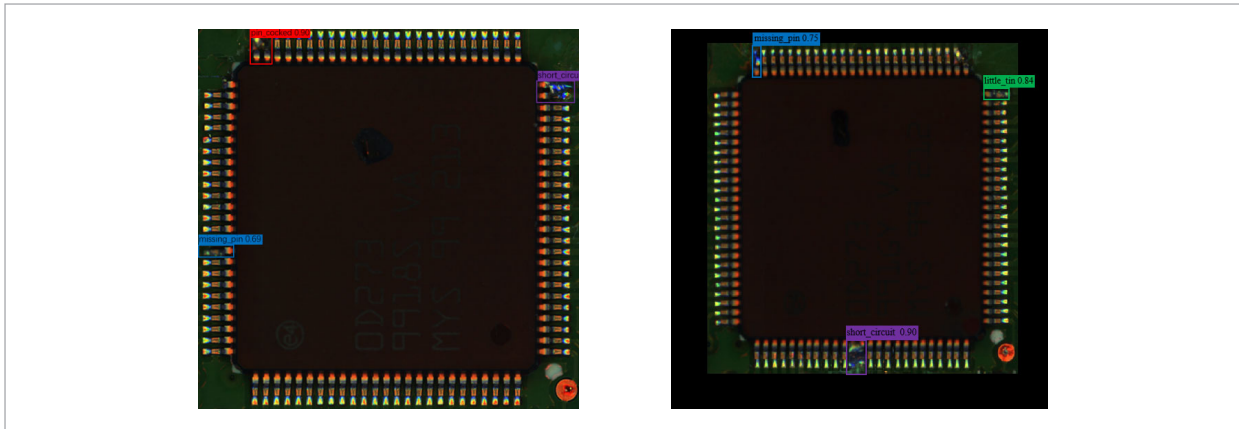


Figure 9

Visualization of detection results of YOLOv5x algorithm

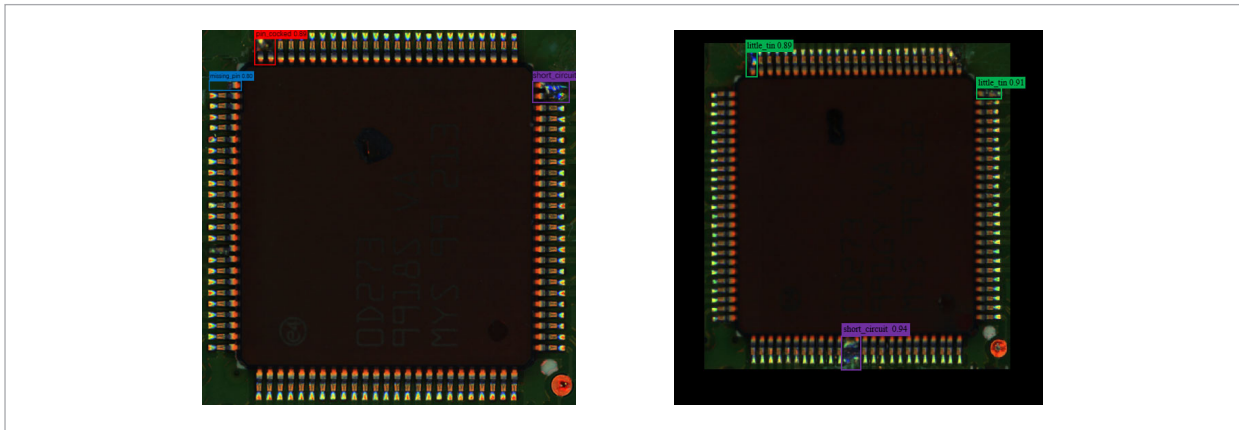


Figure 10

Visualization of detection results of the improved algorithm

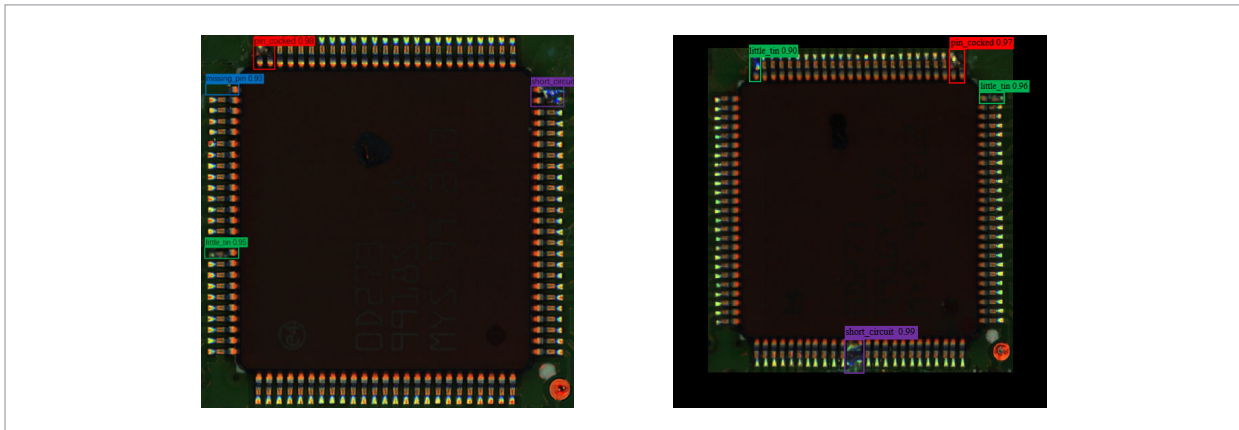


Table 2

Detection results for the left image

Algorithm	Real number of defects	Left image detection results		
		Correct	Missed	False
YOLOv3	4	2	1	1
YOLOv5x	4	3	1	0
Improved	4	4	0	0

Table 3

Detection results for the right image

Algorithm	Real number of defects	Right image detection results		
		Correct	Missed	False
YOLOv3	4	2	1	1
YOLOv5x	4	3	1	0
Improved	4	4	0	0

ly detected one little tin. Similarly, the YOLOv5x algorithm missed one little tin in the left image and one pin cocked in the right image. In contrast, the improved algorithm accurately detected all defects in

both images. These observations collectively demonstrate that the improved algorithm exhibits superior recognition performance for IC pin welding defects when compared to the other two algorithms.

6. Conclusions

This paper presents an IC pin welding defect detection method based on an improved YOLOv5x algorithm. The mAP of the improved algorithm reaches 95.0%, an improvement of 13.3% and 8.9% compared to YOLOv3 and YOLOv5x, respectively. The detection time for a single image using the improved algorithm is 0.142 s, faster than the detection speed of YOLOv3 and YOLOv5x. This work provides new research ideas and methods for IC pin welding defect detection, and has important theoretical and reference value for detecting small and dense targets.

Acknowledgements

Partial financial support was received from Zhejiang province “Jianbing” program project: key technology research and equipment development for high power module device packaging and testing (No.2023C01061).

References

- Cai, N. A., Cen, G. D., Wu, J. X., Li, F. Y., Wang, H., Chen, X. D. SMT Solder Joint Inspection via a Novel Cascaded Convolutional Neural Network. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2018, 8(4), 670-677. <https://doi.org/10.1109/TCPMT.2018.2789453>
- Ding, R. W., Dai, L. H., Li, G. P., Liu, H. TDD-Net: A Tiny Defect Detection Network for Printed Circuit Boards. *CAAI Transactions on Intelligence Technology*, 2019, 4(2), 110-116. <https://doi.org/10.1049/trit.2019.0019>
- Gaidhane, V. H., Hote, Y. V., Singh, V. An Efficient Similarity Measure Approach for PCB Surface Defect Detection. *Pattern Analysis and Applications*, 2018, 21, 277-289. <https://doi.org/10.1007/s10044-017-0640-9>
- Girshick, R., Donahue, J., Darrell, T., Malik, J. Rich Feature Hierarchies for Accurate Object Detection and Semantic Segmentation. *Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, 2014, 580-587. <https://doi.org/10.1109/CVPR.2014.81>
- Girshick, R. Fast R-CNN. *Proceedings of the IEEE International Conference on Computer Vision (ICCV)*, 2015, 1440-1448. <https://doi.org/10.1109/ICCV.2015.169>
- Ibrahim, Z., Khalid, N. K., Ibrahim, I., Abidin, M. S. Z., Mokji, M. M., Bakar, S. A. R. S. A. A Noise Elimination Procedure for Printed Circuit Board Inspection System. *2008 Second Asia International Conference on Modelling & Simulation (AMS)*, 2008, 332-337. <https://doi.org/10.1109/AMS.2008.36>
- Jocher, G., Stoken, A., Borovec, J., Chaurasia, A., Liu, C. Y., Hogan, A., Diaconu, L., Kwon, Y., Defretin, Y., Lohia, A., Milanko, B., Fineran, B., Khromov, D., Ding, Y. W., Ingham, F. Ultralytics/ Yolov5: V5.0- YOLOv5- P6 1280 Models, AWS, Supervise.ly and YouTube Integrations. <https://doi.org/10.5281/zenodo.4679653>
- Kaur, B., Kaur, G., Kaur, A. Detection and Classification of Printed Circuit Board Defects Using Image Subtraction Method. *2014 Recent Advances in Engineering and Computational Sciences (RAECS)*, 2014, 1-5. <https://doi.org/10.1109/RAECS.2014.6799537>

9. Keenan, E., Wright, R. G., Zgol, M., Mulligan, R., Tagliavia, V., Kirkland, L. V. Infrared Laser Imaging for Circuit Board and IC Failure Detection. *Proceeding of IEEE Systems Readiness Technology Conference, 2003*, 399-405. <https://doi.org/10.1109/AUTEST.2003.1243604>
10. Kumar, M., Singh, N. K., Kumar, M., Vishwakarma, A. K. A Novel Approach of Standard Data Base Generation for Defect Detection in Bare PCB. *International Conference on Computing, Communication & Automation, 2015*, 11-15. <https://doi.org/10.1109/CCAA.2015.7148363>
11. Lin, Q. Q., Zhou, J. Z., Ma, Q. R., Ma, Y. J., Kang, L., Wang, J. J. EMRA-Net: A Pixel-Wise Network Fusing Local and Global Features for Tiny and Low-Contrast Surface Defect Detection. *IEEE Transactions on Instrumentation and Measurement, 2022*, 71, 1-14. <https://doi.org/10.1109/TIM.2022.3151926>
12. Lin, T. Y., Dollar, P., Girshick, R., He, K. M., Hariharan, B., Belongie, S. Feature Pyramid Networks for Object Detection. *Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR), 2017*, 2117-2125. <https://doi.org/10.1109/CVPR.2017.106>
13. Liu, S., Qi, L., Qin, H. F., Shi, J. P., Jia, J. Y. Path Aggregation Network for Instance Segmentation. *Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR), 2018*, 8759-8768. <https://doi.org/10.1109/CVPR.2018.00913>
14. Liu, W., Anguelov, D., Erhan, D., Szegedy, C., Reed, S., Fu, C. Y., Berg, A. C. SSD: Single Shot Multi-Box Detector. *European Conference on Computer Vision, 2016*, 21-37. https://doi.org/10.1007/978-3-319-46448-0_2
15. Liu, Y. C., Wang, P., Wang, H. T. Target Tracking Algorithm Based on Deep Learning and Multi-Video Monitoring. *2018 5th International Conference on Systems and Informatics (ICSAI), 2018*, 440-444. <https://doi.org/10.1109/ICSAI.2018.8599349>
16. Luo, J. X., Yang, Z. Y., Li, S. P., Wu, Y. L. FPCB Surface Defect Detection: A Decoupled Two-Stage Object Detection Framework. *IEEE Transactions on Instrumentation and Measurement, 2021*, 70, 1-11. <https://doi.org/10.1109/TIM.2021.3092510>
17. Park, J. Y., Hwang, Y., Lee, D., Kim, J. H. MarsNet: Multi-Label Classification Network for Images of Various Sizes. *IEEE Access, 2020*, 8, 21832-21846. <https://doi.org/10.1109/ACCESS.2020.2969217>
18. Ran, G. Z., Lei, X., Li, D. S., Guo, Z. L. Research on PCB Defect Detection Using Deep Convolutional Neural Network. *2020 5th International Conference on Mechanical, Control and Computer Engineering (ICMCCE), 2020*, 1310-1314. <https://doi.org/10.1109/ICMCCE51767.2020.00287>
19. Redmon, J., Divvala, S., Girshick, R., Farhadi, A. You Only Look Once: Unified, Real-Time Object Detection. *Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR), 2016*, 779-788. <https://doi.org/10.1109/CVPR.2016.91>
20. Redmon, J., Farhadi, A. YOLOv3: An Incremental Improvement. *arXiv preprint arXiv:1804.02767*. 2018.
21. Ren, S. Q., He, K. M., Girshick, R., Sun, J. Faster R-CNN: Towards Real-Time Object Detection with Region Proposal Networks. *IEEE Transactions on Pattern Analysis and Machine Intelligence, 2017*, 39(6), 1137-1149. <https://doi.org/10.1109/TPAMI.2016.2577031>
22. Shen, F. Y. Research on Defect Detection Technology of PCB Bare Board Based on Deep Learning. Chengdu, Sichuan: Xihua University, 2021. <https://doi.org/10.27411/d.cnki.gscgc.2020.000395>
23. Sun, Q., Liu, J. J., Hu, B. B. Research on Integrated Circuit Industry Chain and Innovation Chain Integration Development in China. *Studies in Science of Science, 2023*, 41(07), 1223-1233+1281. <https://doi.org/10.16192/j.cnki.1003-2053.20221011.002>
24. Tang, B., Kong, J. Y., Wu, S. Q. Review of Surface Defect Detection Based on Machine Vision. *Journal of Image and Graphics, 2017*, 22(12), 1640-1663.
25. Vaswani, A., Shazeer, N., Parmar, N., Uszkoreit, J., Jones, L., Gomez, A. N., Kaiser, L., Polosukhin, I. Attention is All You Need. *arXiv preprint arXiv:1706.03762*. 2017.
26. Wang, C. Y., Liao, H. Y., Wu, Y. H., Chen, P. Y., Hsieh, J. W., Yeh, I. H. CSPNet: A New Backbone that can Enhance Learning Capability of CNN. *Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR), 2020*, 390-391. <https://doi.org/10.1109/CVPRW50498.2020.00203>
27. Wang, H. Y., Guo, L. L. Research on Face Recognition Based on Deep Learning. *2021 3rd International Conference on Artificial Intelligence and Advanced Manufacture (AIAM), 2021*, 540-546. <https://doi.org/10.1109/AIAM54119.2021.00113>
28. Wu, Y. Q., Zhao, L. Y., Yuan, Y. B., Yang, J. Research Status and the Prospect of PCB Defect Detection Algorithm Based on Machine Vision. *Chinese Journal of Scientific Instrument, 2022*, 43(08), 1-17. <https://doi.org/10.19650/j.cnki.cjsi.J2209701>

29. Yamada, S., Iwahara, M., Fukuda, Y., Taniguchi, T., Wakawaka, H. Inspection of Bare Printed Circuit Board Using Planar Type ECT Probe. AIP Conference Proceedings, 2004, 374-381. <https://doi.org/10.1063/1.1711647>
30. Zhai, J. B., Chen, J., Qin, Z. F. Common Problems and Corrective Measures in Factory Inspection of Printing Processes of Electronic Products. China Quality Certification, 2022, 06, 73-75. <https://doi.org/10.16691/j.cnki.10-1214/t.2022.06.009>
31. Zhang, H. D., Chen, Z. Z., Zhang, C. Q., Xi, J. T., Le, X. Y. Weld Defect Detection Based on Deep Learning Method. 2019 IEEE 15th International Conference on Automation Science and Engineering (CASE), 2019, 1574-1579. <https://doi.org/10.1109/COASE.2019.8842998>



This article is an Open Access article distributed under the terms and conditions of the Creative Commons Attribution 4.0 (CC BY 4.0) License (<http://creativecommons.org/licenses/by/4.0/>).