ITC 3/47
Journal of Information Technology and Control
Vol. 47 / No. 3 / 2018
pp. 521-531
DOI 10.5755/j01.itc.47.3.19753

Analogue Integrated Circuits Design-for-Testability Flow Oriented onto OBIST Strategy

Received 2017/12/22 | Accepted after revision 2018/08/03

http://dx.doi.org/10.5755/j01.itc.47.3.19753

Analogue Integrated Circuits Design-for-Testability Flow Oriented onto OBIST Strategy

Sergey Mosin

Institute of Computational Mathematics and Information Technologies; Kazan Federal University; Kremlyovskaya str., 18, 420008, Kazan, Russian Federation

Corresponding author: smosin@ieee.org

Oscillation Built-In Self-Test (OBIST) strategy allows to avoid the using complex, expensive generators of input test signals during testing, and uses the oscillation frequency generated at the output of the circuit after reconfiguring into oscillator as a controlled parameter. There configuration subcircuit forms an oscillator from the original circuit in the test mode and requires an additional but insignificant area of the chip, especially against the background of stable increasing the scale of integration for the state-of-the-art integrated technologies. Selection of the efficient type of reconfiguration the original circuit into oscillator and implementation of corresponding test circuitry are the most important tasks, which, as rule, are solved nowadays based on experience of designers without automation and therefore restrict to wide use of the OBIST concept. The paper is mainly focused on the task of design-for-testability (DFT) automation with emphasis on the OBIST strategy for analog integrated circuits (IC). The design procedures according to DFT flow are proposed. Three possible structural solutions for reconfiguration of original circuit into an oscillator are considered. The necessary conditions for stability analysis of reconfigured circuit are presented. The stage of a numerical estimating the transient time before the steady-state operation after reconfiguration of original circuit into an oscillator ensuring definition of the start time point for correct calculating the oscillation frequency is proposed. The set of rules for each structural solution for reconfiguration is prepared as the formal procedures, which can support the automation during the DFT flow. The efficiency of the proposed DFT flow is demonstrated for analog circuits, for which the reconfiguration subcircuits were obtained in an automated way during design-for-testability, as well as the fault simulation has been performed. The experimental results for all cases showed the adequacy of oscillation frequency for revealing both catastrophic and parametric faults. Fault coverage for considered set of faults has consisted up to 100 %.

KEYWORDS: Oscillation-BIST, Analogue circuits, Design automation, Design-for-testability flow, Reconfiguration circuitry.

1. Introduction

Analog and mixed-signal circuits, especially integrated circuits, stipulate a set of challenging issues from the testing point of view. There are at least two main problems in analog testing, firstly, a limited access to internal nodes and, secondly, a complicated selection of test signal(s), which can provide required test quality and fault coverage.

The inclusion of additional test nodes improves the test quality and resolution ability of diagnosis. Nevertheless, the total area of an integrated circuit is increased due to implementation of additional pads and connection lines. As result, the IC package with a greater number of pins and bigger volume of cavity is required. Such a solution leads to increasing the power consumption and raising both the size of IC and the cost of implementation and manufacturing.

Many problems of a test organization can be overcome using Built-In Self-Test (BIST) structural solutions implemented in the framework of Design-for-Testability (DFT) concept [11, 12]. The BIST-solutions are placed on a chip together with original circuit for the purpose of test signal generation, acquisition of the output responses and decision-making about the correctness of operating the circuit under test (CUT). The BIST-circuitries are developed at early stages of IC design process what ensures selecting the most efficient conditions and mechanisms for further high-quality testing the CUT.

The efficient test method that does not need the input test signal and relies on in-circuit implementation was proposed in [1] and called the Oscillation Built-In Self-Test (OBIST). The main idea of this method is a transformation of the original circuit into the oscillator during the test mode and consideration the oscillation frequency (f_{OSC}) as a measured parameter, which depends on the components parameters of the CUT.

The works of many authors suggest the applications and particular developments of the OBIST method from [1], for example. The approach to optimal f_{OSC} generation by changing passive component parameters for covering hard-detectable short faults in analog circuits is proposed in [2]. An application of oscillation-based test to analog filters is considered in [4] emphasizing the layout simulation. Adaptation of the OBIST for analog and mixed-signal embedded core-based system-on-a-chip circuits is presented in [5]. The method based on partition of a high-order Operational Transconductance Amplifier-C filter into second-order filters, which reconfigured into a quadrature oscillator is considered in [6]. The oscillation-based test is proposed in [7] for transforming analog signal into digital one for structural testing the complex mixed-signal macrocells. Kač and Novak [9] offered the approach to transformation of switched-capacitor filter stages for oscillation-based testing. The pulses of oscillating output signals are used in [10] for generating the signature, harnessed for the fault detection. Oscillation-based test is applied in [16] to the second-generation Current Conveyor (CCII) based filters as a case study. Oscillation-based diagnosis using artificial neural network for fault dictionary construction is proposed in [18]. The combination of oscillation-based test strategy with supply current monitoring, is considered in [19] as an alternative to the specification-based test of analog circuits. So, the solutions based on OBIST-strategy and proposed by different authors [2-10, 16, 18-19] demonstrate high efficiency of detection both catastrophic and parametric faults. However, proposed solutions ensure the particular approaches to reconfiguration based on designer's experience. The application-specific approach to selecting a reconfiguration circuit limits the wide use of OBIST. Therefore, OBIST-circuitry design automation fulfilled within the framework of a design-for-testability flow is important step to enhancement of the oscillation-BIST application for efficient testing the different classes of analog and mixed-signal circuits.

This paper is an extended version of work published in [14]. The previous work is extended by detailed specification of two stages concerning with stability analysis and steady-state time estimation for reconfigured circuit, as well as representing the new results. The rest part of the paper is organized as follows. The design-for-testability flow based on the OBIST strategy for analog circuits is presented in Section 2. The concept of reconfiguration circuitry selection and three types of structural solutions are proposed in Section 3. The issues of stability analysis of reconfigured

circuit are considered in Section 4. The approach to numerical estimation of a steady-state time for reconfigured circuit is discussed in Section 5. Section 6 provides describing the rules of reconfiguration for proposed structural solutions. The results of practical experiments are presented in Section 7.

2. Description of the Design-for-Testability Flow Oriented onto the OBIST Strategy

The test method based on reconfiguration into an oscillator uses the oscillation frequency (f_{OSC}) for decision-making about the correctness of original circuit. The f_{OSC} for the fault-free circuit is considered as the reference frequency and estimated during the design stage. The f_{OSC} for CUT, which measured without application of any input test signals, is compared with the reference frequency. OBIST can be realized only in dedicated test mode when the original circuit is reconfigured into oscillator by activation of the test mode select signal. The obtained oscillator generates a periodic signal with eigenfrequency, which depends on parameters of internal circuit components. Any defect provides a deviation of component parameters from the nominal values and has an influence on a change of the eigenfrequency of the circuit under reconfiguration. So, the difference between the reference frequency and oscillation frequency of CUT is a criterion for the fault detection.

The approach to design-for-testability of analog circuits based on the oscillation-BIST strategy is proposed for the automation purpose (Fig. 1). The main idea is connected with implementation of procedures, which provide a selection in automated mode the appropriate configuration circuit and calculation of oscillation frequency band taking into account the components tolerances. The decomposition of the corresponding design flow includes the following steps:

1. Selection of the reconfiguration circuitry for OBIST, which ensures the guaranteed transformation of the original analogue circuit into an oscillator in the test mode.
2. Stability analysis of a reconfigured circuit proves that the circuit will be invariably oscillating after reconfiguration. Adaptation of the current reconfiguration circuitry or selection of an alternative one should be done if the condition of reliable instability after transformation is not achieved.
3. Estimation of the transient time before steady-state operating of the reconfigured circuit allows defining the initial time point of a beginning the regular oscillations. This value is a minimum time delay for oscillation frequency acquisition after switching on the test mode.
4. Calculation of the f_{OSC} for nominal parameters of the circuits' internal components in the form of reciprocal proportion to the period of generated signal.
5. Estimation of the f_{OSC} band taking into account the components tolerances. The Monte-Carlo method is used for calculation such statistical characteristics of oscillation frequency as distribution, mean and deviations, which are used for definition of the confidence interval with required reliability (γ) $[f_{OSC}^{\min}, f_{OSC}^{\max}]_{|\gamma=\text{const}}$.
6. Calculation ot a fault coverage using the results of faults simulation. The specified set of faults, which includes catastrophic and parametric faults, is used for simulation their influence on the oscillation frequency

$$\mathbf{FS} = \mathbf{FSc} \cup \mathbf{FSp}\,, \tag{1}$$

where **FSc** is a finite subset of catastrophic faults, **FSp** is an infinite subset of parametric faults. The quantity and type of parametric faults are selected for each circuit individually providing reasonable completeness of estimating the circuit behavior.

7. Physical measurement of oscillation frequency for the circuit-under-test (CUT) – f_{OSC_CUT}.
8. Comparison of measured f_{OSC_CUT} with bounds on the frequency band and decision-making about CUT status

$$f_{OSC}^{\min} \le f_{OSC\_CUT} \le f_{OSC}^{\max}\,. \tag{2}$$

If Condition (2) is true, the CUT is considered as fault-free, otherwise as faulty.

Steps 1-6 correspond to Simulation-before-Test (SBT) concept. Steps 7-8 are performed for each CUT during the functional testing stage.

3. Selection of the Reconfiguration Circuitry for the Oscillation BIST

Mainly, the *OBIST* strategy is used in off-line mode and success of faults detection depends on the way of original circuit reconfiguration into oscillator. The task of selecting a proper reconfiguration circuitry can be formalized in design-for-testability flow and solved in an automated mode.

The approach is illustrated by an example of active filters. The second order transfer function used for description of filter's behavior is the following:

$$\frac{V_{out}(s)}{V_{in}(s)} = K\frac{s^2+(\omega_z/Q_z)s+\omega_z^2}{s^2+(\omega_p/Q_p)s+\omega_p^2}, \quad (3)$$

where ω_z and ω_p are eigenfrequencies of zeros and poles, Q_z and Q_p are values of Q-factor for zeros and poles.

The poles of the transfer function can be expressed from Equation (3) in terms of ω_p and Q_p:

$$p_{1,2} = \sigma \pm j\omega = -\frac{\omega_p}{2Q_p} \pm j\frac{\omega_p}{2Q_p}\sqrt{4Q_p^2-1}\,. \quad (4)$$

The poles must be situated on the imaginary axes $j\omega$ in order for the circuit to provide a signal generation at resonant frequency ω_p with constant amplitude. According to Equation (4) this condition is held true when $Q_p \to \infty$.

Both values ω_p and Q_p depend on parameters of internal circuit's components. The circuitry ensuring enough high value for Q-factor at unchangeable value of resonant frequency should be selected as a solution for original circuit reconfiguration for providing the stable oscillation, i.e.

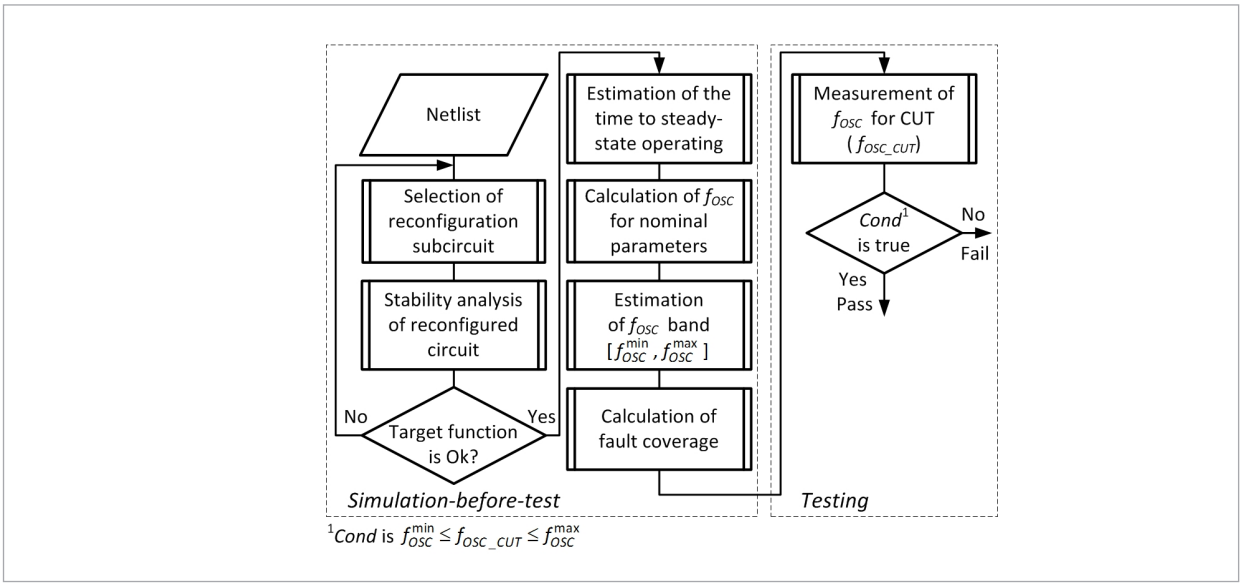
$$\omega_p(\mathbf{p_1}) = const, Q_p(\mathbf{p_2}) \to \infty \,|\, \exists \tilde{\mathbf{p}}, \quad \mathbf{p_1} \cap \tilde{\mathbf{p}} = 0, \mathbf{p_1} \subseteq \mathbf{p}, \mathbf{p_2} \subseteq \mathbf{p}, \quad (5)$$

where $\tilde{\mathbf{p}}$ is a set of parameters for circuit's internal components changing in the testing mode, $\mathbf{p}$ is a set of parameters for circuit's internal components.

The following structural solutions for the circuit reconfiguring into an oscillator providing condition from Equation (5) are proposed:

1. Disconnection of internal lines by switches.
2. Forming of required gain factor for an active nonlinear element by plug-in extra components.
3. Inclusion of additional feedback(s).

Figure 1
Design-for-testability flow oriented onto Oscillation Built-In Self-Test



The selection of the way and particular circuits for reconfiguration of the original device is performed during design stage. The different variants of reconfiguration into an oscillator are considered taking into account specific of the original circuit. The criterion of selection is the maximum of instability factor for the oscillator in test mode among k considered ways:

$$\arg\max_i\left(Instab_i\right), \forall i = 1..k\,, \tag{6}$$

where $Instab_i$ is instability factor for the circuit reconfigured by the i-th way.

The factors for all variants may be estimated simultaneously in a CAD tool using parallel paradigm for multicores or multiprocessors computer workstation [13], [15].

4. Stability Analysis of the Reconfigured Circuit

An oscillator obtained after reconfiguration of the original circuit consists of frequency-dependent subcircuit and active nonlinear element comprised by a feedback.

The following condition called as the Barkhausen stability criterion should be provided in order to ensure oscillation [17]

$$A\beta = -1\,, \tag{7}$$

where A is the gain of active nonlinear element, β is the transfer function of the feedback path.

The loop gain around the feedback path has to coincide in phase with corresponding phase shift equal to 180°. The condition (7) has the following form depending on the application either positive (8) or negative (9) feedback

$$|A||\beta| = 1\angle -0^\circ\,, \tag{8}$$

$$|A||\beta| = 1\angle -180^\circ. \tag{9}$$

The necessary amplitude condition for oscillation is the compensation of the attenuation in the feedback loop by the active nonlinear element.

The necessary phase condition for oscillation is coincidence of phases for output and input signals.

The Nyquist stability criterion based on estimation of the amplitude-phase characteristic in complex plane can also be used for the stability analysis.

5. Estimation of Time to Steady-State Operating of the Reconfigured Circuit

The reactive and nonlinear elements in the analog circuit provide the transient processes before the steady-state regime of operation.

The transient and steady-state processes in the reconfigured circuit are simulated in the time mode using the transient analysis. The indirect form of the circuit representation is used for mathematical description of the oscillator model

$$F_i\left(\frac{dx(t)}{dt}, \int x(t)\,dt, x(t)\right) = 0\,,\ i = 1..p\,. \tag{10}$$

The finite-difference approximations corresponding to numerical differentiation (f_D) and integration (f_I) are used for solving the system of Equations (10)

$$\frac{dx(t)}{dt} \approx f_D\left(x_{n+1}, x_n, ..., x_{n-k}\right); \tag{11}$$

$$\int_a^b x(t)dt \approx f_I\left(x_{n+1}, x_n, ..., x_{n-k}\right). \tag{12}$$

The finite-difference algebraic equations are formed by substituting the Equations (11) and (12) into the system of Equations (10)

$$F_i\left(x_{n+1}, x_n, ..., x_{n-k}\right) = 0\,,\ i = 1..p\,. \tag{13}$$

The obtained model (13) is solved concerning x_{n+1} by a numerical method of solving the finite equations. When x_{n+1} is calculated with specified accuracy, the calculated time points are shifted on the one step considering $x_n = x_{n+1}$, $x_{n-1} = x_n$, etc. and the system of Equations (13) is solved again concerning new value

x_{n+1}. This process is repeated until the final time point t is reached.

The time point of starting the stable oscillation t_{ss}^0 corresponding to the duration of the transient processes before the steady-state operating is calculated based on solving the system of Equations (13).

The steady-state process in oscillator is periodical with the following appropriate condition:

$$x\left(t_{ss}^0\right) = x\left(t_{ss}^0 + T\right), \quad (14)$$

where T is the period of oscillating.

6. The Rules of Reconfiguration for Three Proposed Structural Solutions

A. For Disconnection of Internal Lines by Switches

1 Define a transfer factor for the original circuit according to Equation (3).
2 Express ω_p and Q_p by parameters of circuit's internal components.
3 Select the set of independent parameters $\tilde{\mathbf{p}}$ for expressions of ω_p and Q_p.
4 Provide the fulfillment of condition $Q_p \to \infty$ using set $\tilde{\mathbf{p}}$.
5 Include to original circuit the structural solution providing required values for parameters in $\tilde{\mathbf{p}}$ in the test mode.
6 Define the control signals for the normal and test modes.

B. For Forming of Required Gain Factor for an Active Nonlinear Element by Plug-in Extra Components

1 Define a transfer factor for the original circuit according to Equation (3).
2 Express ω_p and Q_p by parameters of circuit's internal components.
3 If the expression for Q_p depends on the gain factor of active nonlinear element covered by feedback and its parameters $\tilde{\mathbf{p}}$ have no influence on ω_p, then calculate values of corresponding parameters providing the fulfillment of condition $Q_p \to \infty$. Parameters $\tilde{\mathbf{p}}$ are calculated by solving the system of equations.
4 Include to original circuit the structural solution providing required values for parameters in $\tilde{\mathbf{p}}$ in test mode.
5 Define the control signals for the normal and test modes.

C. For Inclusion of an Additional Feedback(s)

1 Define a transfer factor for the original circuit according to Equation (3).
2 Estimate the stability of the circuit.
3 Consider the feedback(s) in the original circuit providing instability of the obtained circuit.
4 Include a selected structural solution in the original circuit design, ensuring appearance of the feedback in the test mode.
5 Express the oscillation frequency by parameters of internal circuit and feedback circuit.
6 Define the control signals for the normal and test modes.

7. Experimental Results

The application of rules for structural solution based on disconnection of internal lines is considered for second-order *RC*-filter (Fig. 2, *a*).

The gain function in node 5 corresponds to bandpass filter

$$V_5(s)/V_1(s) = H_0 \omega s / \omega_0^2 + \omega_0 s / Q + s^2. \quad (15)$$

The central frequency and quality factor are described by Equations (16) and (17) correspondingly

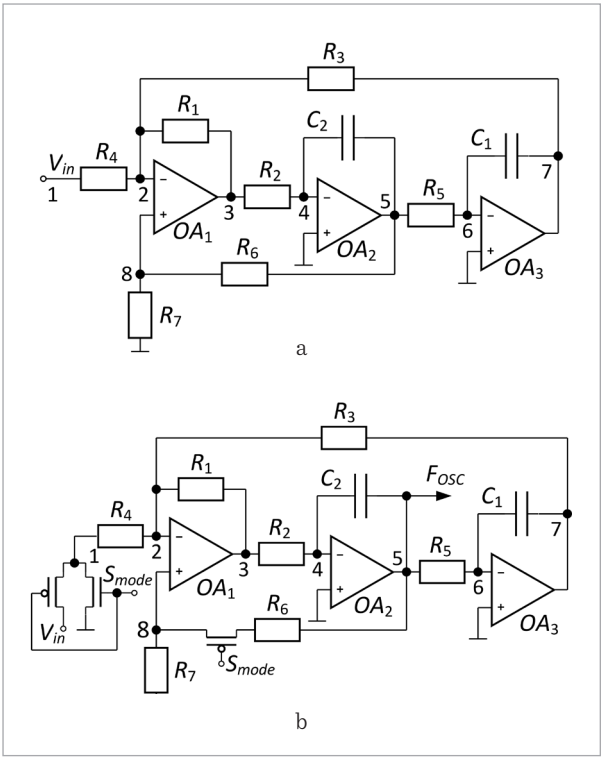
$$\omega_0 = \sqrt{R_1 / \left(R_3 R_2 R_5 C_1 C_2\right)}, \quad (16)$$

$$Q = \left(R_7 / \left(R_6 + R_7\right)\left(1 + R_1\left(R_3 + R_4\right)/\left(R_3 R_4\right)\right)\right)^{-}. \quad (17)$$

The set of independent parameters for Equations (16) and (17) includes $\tilde{\mathbf{p}} = \{R_4, R_6, R_7\}$. The simplest way to ensure the condition $Q_p \to \infty$ using elements from $\tilde{\mathbf{p}}$ is assignment R_6 to infinity. Such an assignment for R_6 can be realized as disconnection of this resistor from node 5 or 8, i.e. open effect ($R_6 \approx \infty$). The use of a MOS-switch in sequence with R_6 ensures the switching on or off the resistor by the test mode signal applied to the gate.

Figure 2

Second-order *RC*-filter: original (*a*), reconfigured (*b*) ($R_1 = R_2 = R_3 = R_4 = R_5 = 10\text{k}\Omega$, $R_6 = 12\text{k}\Omega$, $R_7 = 1\text{k}\Omega$, $C_1 = C_2 = 20\text{nF}$)



The second order *RC*-filter with OBIST-circuitry is depicted in Fig. 2, *b*.

Fault-free and faulty conditions with inclusion of the single catastrophic (hard) and parametric (soft) faults into the filter consist of the set of states. Short circuit and open circuit effects for internal components are considered as the catastrophic faults. The deviations of nominal parameters for internal components of the filter in + 50% and – 50% are used for parametric faults simulation. Fault-free circuit was simulated using Monte-Carlo method with 2 000 iterations. The tolerance of internal parameters is assigned as 10 %. The normal distribution on the range [–1, 1] with zero mean and standard deviation $\sigma = 0.25$ are used for calculating the actual parameters' values for fault-free components at each iteration. The PSpice EDA tool of CADENCE on the computer system Intel® Core™ i7-4770 CPU @ 3.40GHz and RAM 8 GB was used for circuit simulation for all experiments.

The f_{OSC} band for the fault-free behavior was estimated for two values of reliability $\gamma = 0.9$ and $\gamma = 0.98$:

$$f_{OSC} = [753\,\text{Hz}, 827\,\text{Hz}]_{\gamma=0.9}$$

and

$$f_{OSC} = [735\,\text{Hz}, 851\,\text{Hz}]_{\gamma=0.98}.$$

Fault coverage for both values of reliability provides the same results: 87.5 % for the hard faults and 75 % for the soft faults (Table 1).

Table 1

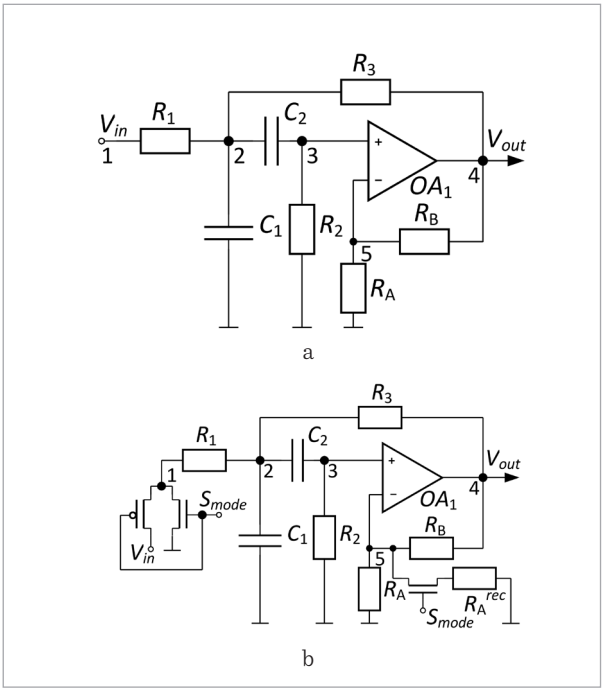
Fault coverage for Second-order *RC*-filter

Parameter	Reliability	
	$\gamma = 0.9$	$\gamma = 0.98$
Number of hard faults	16	16
Number of detected hard fault	14	14
Hard fault coverage, %	87.5	87.5
Number of soft faults	16	16
Number of detected soft fault	12	12
Soft fault coverage, %	75	75

The rules for forming the required gain factor are demonstrated for the Sallen-Key filter (Fig. 3).

Figure 3

Sallen-Key filter: original (*a*), reconfigured (*b*) ($R_1 = R_3 = R_B = 10\text{k}\Omega$, $R_2 = 20\text{k}\Omega$, $R_A = 1\text{k}\Omega$, $C_1 = C_2 = 220\text{nF}$)



The central frequency and quality factor are the following

$$\omega_0 = \sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3 C_1 C_2}}, \tag{18}$$

$$Q = \frac{\sqrt{(R_1 + R_3) R_1 R_2 R_3 C_1 C_2}}{R_1 R_3 (C_1 + C_2) + R_2 C_2 (R_3 - R_1 (K-1))}. \tag{19}$$

Q in (19) depends on the gain factor $K = 1 + R_B / R_A$ and ω_0 does not depend on the resistors R_A and R_B. Therefore

$$Q \to \infty \Rightarrow \frac{1}{Q} = 0, R_1 R_3 (C_1 + C_2) + \\ + R_2 C_2 (R_3 - R_1 (K-1)) = 0, \tag{20}$$

$$K = \frac{R_1 R_3 (C_1 + C_2) + R_2 C_2 (R_1 + R_3)}{R_1 R_2 C_2}. \tag{21}$$

The parameters for reconfiguration circuitry are defined by solving the following system of equations

$$\begin{cases} \dfrac{R_B}{R'_A} = \dfrac{R_1 R_3 (C_1 + C_2) + R_2 C_2 (R_1 + R_3)}{R_1 R_2 C_2} - 1; \\ R'_A = \dfrac{R_A + R_A^{rec}}{R_A R_A^{rec}}, \end{cases} \tag{22}$$

where R'_A is the equivalent resistor in the test mode, R_A^{rec} is the compensating resistor ensuring the condition in the Equation (20).

The Nyquist diagram of a gain in node 4 for original Sallen-Key filter is represented in Fig. 4, *a*. The locus does not comprise the point (–1, *j*) on a complex plane and consequently the original circuit of filter is stable. The Nyquist diagram of a gain for reconfigured circuit of Sallen-Key filter, where R_A has been changed onto equivalent resistor R'_A, is represented in Fig. 4, *b*. In the second case, the locus comprises the point (–1, *j*) on the complex plane and the circuit of filter after reconfiguration is unstable, i.e. provides oscillation.

The results of simulation of the filter operation in the normal mode and after reconfiguration in time domain are shown in Fig. 5. During normal mode the output signal is proportional to the input sine wave in accordance to the transfer function. In the reconfiguration mode,

Figure 4

Nyquist diagram for Sallen-Key filter: original (*a*), reconfigured (*b*)

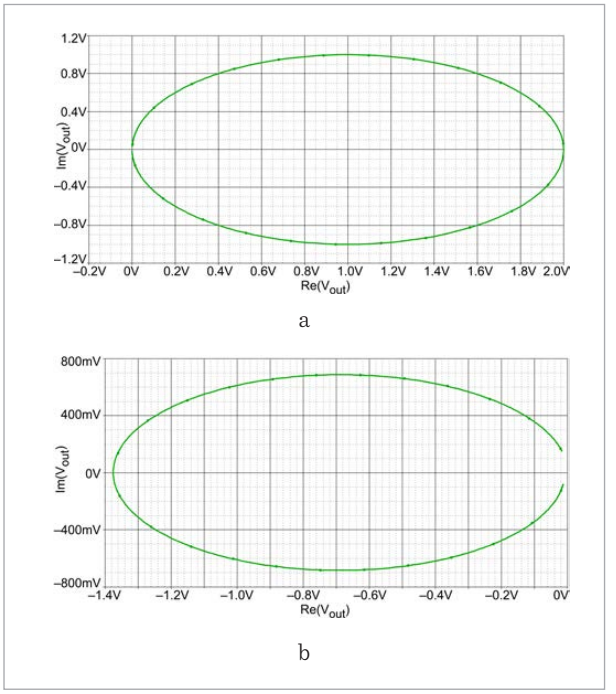
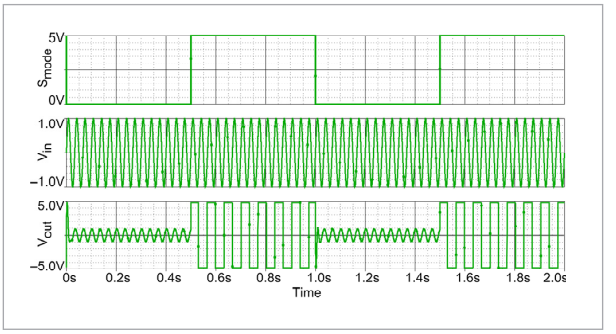


Figure 5

Time domain simulation results for the Sallen-Key filter



the output signal is a periodical sequence of rectangle pulses with constant frequency which depends on components parameters of the filter.

The fault-free and faulty behaviors were simulated with the same parameters as for the second-order *RC*-filter. The f_{OSC} band for fault-free behavior was estimated with different reliability

$$f_{OSC} = [13.9\,\text{Hz}, 15.2\,\text{Hz}]_{\gamma=0.9}$$

and

$$f_{OSC} = [13.5\,\text{Hz}, 15.7\,\text{Hz}]_{\gamma=0.98}.$$

Fault coverage for hard and soft faults for both values of reliability is represented in Table 2.

Table 2
Fault coverage for the Sallen-Key filter

Parameter	Reliability	
	γ = 0.9	γ = 0.98
Number of hard faults	14	14
Number of detected hard fault	11	11
Hard fault coverage, %	78.5	78.5
Number of soft faults	14	14
Number of detected soft fault	9	5
Soft fault coverage, %	64.3	37.5

The rules for the third structural solution based on inclusion of additional feedback(s) are considered for the differentiator circuit (Fig. 6), whose gain factor is the following

$$V_{out}(s)/V_{in}(s) = V_3(s)/V_1(s) = -RCs. \quad (23)$$

The instability required for oscillation is provided by an inclusion of the positive feedback and shortening the input source (Fig. 6, *b*).

The f_{OSC} is calculated using the value of output signal period, whose duration depends on the capacitor recharging processes:

$$-V_s + \left(\frac{R_k}{R_{OC}+R_k}+1\right)V_s e^{-\frac{T/2}{RC}} = -\frac{R_k}{R_{OC}+R_k}V_s, \quad (24)$$

$$T = 2RC\ln\left(1+2R_k/R_{OC}\right), \quad (25)$$

$$f = 1/T = \left(2RC\ln\left(1+2R_k/R_{OC}\right)\right)^{-1}. \quad (26)$$

The f_{OSC} is the function, arguments of which are the parameters of internal components, according to Equation (25). Thus, the reconfiguration circuitry ensures oscillation and influence of original circuit parameters and consequently possible faults onto oscillation frequency value.

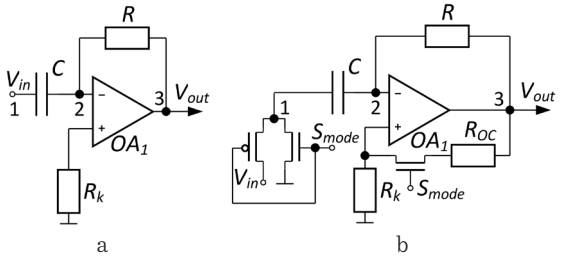
The f_{OSC} band for different reliability and fault coverage were estimated based on simulation of the fault-free and faulty behavior. The f_{OSC} band for fault-free behavior is the following

$$f_{OSC} = [1068\,\text{Hz}, 1375\,\text{Hz}]_{\gamma=0.9} \quad (27)$$

and

$$f_{OSC} = [1000\,\text{Hz}, 1480\,\text{Hz}]_{\gamma=0.98}. \quad (28)$$

Figure 6
Differentiator on the OpAmp: original (*a*), reconfigured (*b*) (R = 10kΩ, R_k = 10kΩ, C = 200nF)



Fault coverage for both cases of hard and soft faults for both values of reliability reaches 100% (Table 3).

Table 3
Fault coverage for the Differentiator

Parameter	Reliability	
	γ = 0.9	γ = 0.98
Number of hard faults	8	8
Number of detected hard fault	8	8
Hard fault coverage, %	100	100
Number of soft faults	8	8
Number of detected soft fault	8	8
Soft fault coverage, %	100	100

The high sensitivity of frequency *f* given by (26) to the deviations caused by the considered catastrophic and parametric faults leads to a significant deviation of the oscillation frequency outside the fault-free band obtained for the reliability values of 0.9 (27) and 0.98 (28) in the case of presence of the corresponding faults in the CUT. Therefore the fault coverage for

both cases attains 100 %. The sensitivity has at least the quadratic dependence on the faulty component deviation, for instance,

$$\partial f / \partial R = -\left(R^2 C \ln\left(1+2R_k / R_{OC}\right)\right)^{-1}, \quad (29)$$

$$\partial f / \partial C = -\left(RC^2 \ln\left(1+2R_k / R_{OC}\right)\right)^{-1}, \quad (30)$$

$$\partial f / \partial R_k = -2\left(R\,C R_{OC} \ln\left(1+2R_k / R_{OC}\right)^2 \times \right. \\ \left. \times\left(1+2R_k / R_{OC}\right)\right)^{-1}. \quad (31)$$

8. Conclusion

Oscillation-BIST strategy provides a useful and efficient mechanism for in-circuit testing and diagnosis of analog and mixed-signal circuits. Selecting the most proper reconfiguration circuit is one of the challenges during practical implementation. Three possible structural solutions proposed in the paper provide transformation of original circuit into oscillator, which generates periodical output signal without application of any input signals, but only power supply. The set of rules for each solution is prepared as the formal step-by-step procedures, which can support the automation during the design-for-testability flow [13].

Experimental results demonstrate the adequacy of the proposed rules for construction of the oscillator after reconfiguring the original circuit, oscillation frequency of which depends on the parameters of internal components. Such a circumstance means that oscillation frequency is sensitive to high and low deviations of the components parameters, i.e. both catastrophic and parametric faults. Therefore oscillation frequency can be used as a controlled parameter for detection of correct or faulty CUT operation and fault diagnosis in the second case. Experimental results show high fault coverage up to 100% for both catastrophic and parametric faults without using special expensive generators of input test signal.

The future research will be carried out in the field of selecting the efficient structural solution for reconfiguration into an oscillator ensuring maximum fault coverage taking into account the components tolerances and considering additional controlled parameters such as an amplitude and phase of output oscillating signal.

Acknowledgement

The work is performed according to the Russian Government Program of Competitive Growth of Kazan Federal University.

References

1. Arabi, K., Kaminska, B. Oscillation Built-In Self-Test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits. Proceedings International Test Conference, 1997, 786-795. https://doi.org/10.1109/TEST.1997.639692
2. Arbet, D., Stopjaková, V., Kováč, M. Investigation of the Optimum Oscillation Frequency Value Towards Increasing the Efficiency of OBIST Approach. Microelectronics Reliability, 2015, 55(7), 1120-1125. https://doi.org/10.1016/j.microrel.2015.03.017
3. Assaf, M. H., Fathi, M. Built-In Hardware for Analog Circuitry Testing. Electronics, Robotics and Automotive Mechanics Conference, CERMA 2008, 14-19. https://doi.org/10.1109/CERMA.2008.7
4. Callegari, S., Pareschi, F., Setti, G., Soma, M. Complex Oscillation-Based Test and Its Application to Analog Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57(5), 956-969. https://doi.org/10.1109/TCSI.2010.2046956
5. Das, S. R., Zakizadeh, J., Biswas, S., Assaf, M. H., Nayak, A. R., Petriu, E. M., Jone, W.-B., Sahinoglu, M. Testing Analog and Mixed-Signal Circuits with Built-In Hardware – A New Approach. IEEE Transactions on Instrumentation and Measurement, 2007, 56(3), 840-855. https://doi.org/10.1109/TIM.2007.894223
6. Hasan, M.-U., Zhu, Y., Sun, Y. Design for Testability of High-Order OTA-C Filters. International Journal of Circuit Theory and Applications, 2016, 44(10), 1859-1873. https://doi.org/10.1002/cta.2200. https://doi.org/10.1002/cta.2200
7. Huertas, G., Vázquez, D., Peralías, E. J., Rueda, A., Huertas, J. L. Testing Mixed-Signal Cores: A Practical

Oscillation-Based Test in an Analog Macrocell. IEEE Design and Test of Computers, 2002, 19(6), 73-82. https://doi.org/10.1109/MDT.2002.1047746

8. Jang, E. J., Gattiker, A., Nassif, S., Abraham, J. A. An Oscillation-Based Test Structure for Timing Information Extraction. Proceedings of the IEEE VLSI Test Symposium, 2012, 74-79. https://doi.org/10.1109/VTS.2012.6231083
9. Kač, U., Novak, F. Practical Considerations in Oscillation Based Test of SC Biquad Filters. Information Technology and Control, 2014, 43(1), 28-36. https://doi.org/10.5755/j01.itc.43.1.3893
10. Khade, R. H., Chaudhari, D. S. OBIST Methodology Incorporating Modified Sensitivity of Pulses for Active Analogue Filter Components. International Journal of Electronics, 2018, 105(3), 457-472.https://doi.org/10.1080/00207217.2017.1376712
11. Milor, L. A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing. IEEE Transactions on Circuits and Systems II, 1998, 45(10), 1389-1407. https://doi.org/10.1109/82.728852
12. Mosin, S. G. Structural Solutions on Design-for-Testability of the Application Specific Integrated Circuits. Information technologies, 2008, 11, 2-10.
13. Mosin, S. G. Design-for-Testability Automation of Mixed-Signal Integrated Circuits. Proceedings of IEEE 26th International SOC Conference (SOCC 2013), 2013, 244-249. https://doi.org/10.1109/SOCC.2013.6749695
14. Mosin, S. An Approach to Design-for-Testability Automation of Analogue Integrated Circuits Using OBIST Strategy. Proceedings of 5th Mediterranean Conference on Embedded Computing (MECO), Bar, Montenegro, 2016, 211-214. https://doi.org/10.1109/MECO.2016.7525742
15. Mosin, S. Automated Simulation of Faults in Analog Circuits Based on Parallel Paradigm. 2017 IEEE East-West Design & Test Symposium (EWDTS), Novi Sad, Serbia, 2017, 1-6. https://doi.org/10.1109/EWDTS.2017.8110133
16. Petrashin, P., Toledo, L., Lancioni, W., Osuch, P., Stander, T. Oscillation-Based Test in a CCII-Based Bandpass Filter. 2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS), 2017, 1-4. https://doi.org/10.1109/LASCAS.2017.7948042
17. Stofanik, V., Minarik, M., Brezovic, Z., Balaz, I., Kudjak, V. Comparison of Classical and Modified Wien Oscillator Circuits in Term of Existence of Steady State Oscillations. 24th International Conference Radioelektronika (RADIOELEKTRONIKA), 2014, 1-4. https://doi.org/10.1109/RadioElek.2013.6530906
18. Stošović, M. A., Milić, M., Zwolinski, M., Litovski, V. Oscillation-Based Analog Diagnosis Using Artificial Neural Networks Based Inference Mechanism. Computers & Electrical Engineering, 2013, 39(2), 190-201. https://doi.org/10.1016/j.compeleceng.2012.12.006
19. Suenaga, K., Isern, E., Picos, R., Bota, S., Roca, M., García-Moreno, E. Application of Predictive Oscillation-Based Test to a CMOS OpAmp. IEEE Transactions on Instrumentation and Measurement, 2010, 59 (8), 2076-2082. https://doi.org/10.1109/TIM.2009.2031381