PROPERTIES OF VARIABLE N-DETECTION FUNCTIONAL DELAY FAULT TESTS

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Abstract. The analysis how the functional fault tests detect structural faults at gate-level shows that the stuck-at fault coverage is much higher than transition fault coverage. The aim of the paper is to discover the reasons of this phenomenon and to propose the techniques of functional delay test quality improvement. We suggest, by transformation of pin pair test into functional delay test, to use variable number of fault detections. The performed experiments show the effectiveness of the introduced approach.

1. Introduction

The main objective of traditional test development has been the achievement of high stuck-at fault coverage. The increasing design complexity and reduced error margins in semiconductor manufacturing are forcing design and test engineers to take a new look at fault models. Rapidly shrinking feature sizes raise the spectrum of new types of defects, and increasing gate counts have increased the number of locations where such defects can occur. The presence of some random defects does not affect a circuit's operation at slow speed while it may cause circuit malfunction at rated speed. This kind of defect is called the delay defect. With ever shrinking geometries, growing density and increasing clock rate of chips, delay testing is gaining more and more industry attention to maintain test quality for speed-related failures. The purpose of a delay test is to verify that the circuit operates correctly at a desired clock speed. Although application of stuck-at fault tests can detect some delay defects, it is no longer sufficient to test the circuit for the stuck-at faults alone. Therefore, delay testing is becoming a necessity for today's integrated circuits.

Three classical fault models are developed to represent delay defects (transition fault, gate delay fault, path delay fault) [1]. Sometimes there is used the fourth type of delay fault model – segment delay fault, which is intermediate to the gate delay and path delay faults. All these fault models have their advantages and weaknesses. The most different models among them are transition fault model and path delay model. On one hand, transition fault patterns are considered to be more effective for large size delay defects, which can happen randomly at any site of a circuit. On the other hand, path delay test patterns aim to detect small size delay defects on a selected set of long timing paths. It is then hoped that the combination of these two orthogonal strategies can capture most of the delay defects and ensure the circuit performance.

In the case when a gate-level description of the Circuit-Under-Test (CUT) is not available, functional-level test generation must be performed. A test set generated at the functional level is independent of and effective for any implementation and, therefore, can be generated at early stages of the design process [2, 3]. Another advantage of functional ATPG for delay faults over structural ATPG is related to the number of targeted faults. For structural ATPG, the number of faults is proportional to the number of paths in the circuit, which very often is exponential in circuit size. In the case of functional ATPG, the number of targeted faults is only proportional to the product of the number of inputs and the number of outputs in the circuit [3].

The analysis how the functional fault tests detect structural faults at gate-level is presented in the papers [4, 5]. The same test generation method was used for development of 1-detection functional static fault [4] and delay [5] tests. The published results show that the stuck-at fault coverage (99.5%) is much higher than transition fault coverage (95.8%). Thus naturally there raises the question why these fault coverages so differ. The aim of the paper is to discover the reasons of aforementioned phenomenon and to propose the possibilities of functional delay test quality improvement.

The paper is organized as follows. We review the related work in Section 2. We analyze the applying of functional tests for structural fault detection in Section 3. We present the experimental results in Section 4. We finish with conclusions in Section 5.

2. Related work

Under functional delay fault models proposed in [6-8], a fault is a tuple (I, O, t I, t O), where I is a CUT input, O is a CUT output, t I is a rising or falling transition at I , and t O is a rising or falling transition at O. Thus, four functional delay faults are associated with every input/output (I/O) pair and the total number of faults is 4*n*m, where n is the number of inputs of the CUT and m is the number of outputs of the CUT. A test for the functional delay fault is a pair of input patterns <u, v> that propagates a transition from a primary input to a primary output of a circuit [3]. Under the model introduced in Underwood et al. [6], only one pair of test patterns must be generated per fault. This model was expanded in Pomeranz and Reddy [8] by considering Δ different test patterns per fault. Δ is a positive integer, usually in the low hundreds, and is given as an input parameter for each CUT. Pomeranz and Reddy [7] proposed that all possible patterns are generated for each fault. This model guarantees detection of all robustly testable path delay faults in any gate-level implementation. However, the resulting sizes of the test sets as well as the test generation times are very large and make this model impractical, especially for large circuits [7, 8]. However, the studies in [8] showed that it is not necessary to generate all possible test patterns for each fault in order to guarantee that actual path delays are covered in some gate-level implementation of the function. The validity of the model in Pomeranz and Reddy [8] is verified by applying the generated test sets to various gate-level implementations [3, 8].

Another fault model for functional ATPG based on input-output stuck-at faults testing, called pin pair (PP) fault model, is suggested by Bareiša et al. in [9] and generalized in [4]. The pin fault model considers the stuck-at-0/1 faults occurring at the module boundary, and has a weak correlation with the circuit's physical faults. We write x_i^1 and x_i^0 for the input stuck-at-1/0 faults, and z_j^1 and z_j^0 for the output stuck-at-1/0 faults. There are 2*n+2*m possible pin faults. Input-output pin stuck-at fault pairs (x_i^t, z_j^k), t=0,1, k=0,1 are called pin pair faults (PP). The number of possible pin pair faults of the circuit is at most 4*n*m.

The methods for deriving the functional delay fault test from PP fault test are described in [10, 11]. Every from PP tests according to approach [10] composed test pair is single-input transition test (SIT) [3] and, therefore, every test pair propagates the transition from a primary input to a primary output in a function robust manner [3]. Another observation is that the test generation for PP faults can be accomplished using various approaches: 1. One test is generated for each PP fault in the circuit; 2. All possible tests are generated for each PP fault in the circuit; 3. Δ tests are generated for each PP fault in the circuit. Thus the functionnal delay tests obtained from PP tests generated using approaches 1, 2 or 3 correspond to tests generated using models described in [6], [7] and [8], respectively.

In the paper [11], there are defined the necessary conditions for the transition propagation from the considered input to considered output in the multi-input transition test (MIT) [3] pattern pair. It is proved that the test pattern pairs composed according to these conditions guarantee function-robustly propagation of signal value transition on the input to the output. On this basis, there is developed a functional PP fault test transformation into functional delay test procedure that allowed improving test compaction. The obtained test is MIT test, and one test is generated for each PP fault in the circuit.

The possibilities of test quality enhancement using the n-detection test set are analyzed in [12, 13]. The n-detection test set is one where each fault f is detected by n different input patterns or by the maximum number of input patterns if f has fewer than n different input patterns that detect it. Pomeranz and Reddy [12] have proposed a reordering procedure to obtain n-detection test sets and variable n-detection test sets for transition faults. Takahashi [13] applies n-detection test sets to check path delay faults where n is a function of the number of paths through the check points.

3. Application of functional tests for structural fault detection

The testing engineer prepares the functional test according to the specification of the device. The functional test is used to verify the next steps of the design and it can be used for the development of the manufacturing test as well. Such a test usually verifies the function of the device and it cannot guarantee the full coverage of the structural faults at the gate level of the device. Therefore if we plan to use the functional test for detection of structural level faults, we have to find means how to increase the quality of functional test.

The investigations show that the 1-detection static functional tests generated for PP faults detect on the average 99.5% stuck-at faults [4]. Such a fault coverage is acceptable even for manufacturing test. However the 1-detection functional delay tests that are derived from the same PP fault tests using methods described in [10, 11] detect on the average just 96% gate-level transition faults [5]. The fault coverage difference is substantial and we found out the reasons of this occurrence.

In case of 1-detection functional delay fault test, every fault is detected only once, i. e. only one test pattern pair detects particular functional delay fault. The same approach is used also for PP fault test generation. If considered input pattern detects at least one new (not yet detected on generated test set) PP fault, this pattern is included into test set. However in contrast to functional delay fault detection the considered test pattern detects not only targeted PP fault

but also other PP faults that are detected by patterns already included into the test set. Let's say that input pattern *r1* detects PP faults {a, b, c, d, e} whereas input pattern *r2* detects the following PP faults {b, c, f, g}. Both input patterns are included into test set and this test set will detect the PP faults {b, c} twice. Therefore there exists a possibility that, at the structural circuit description level, the PP fault *b* and/or *c* detection on test pattern *r2* will occur using different as on the test pattern *r1* signal propagation from input to output paths and thus additional stuck-at faults will be detected. Whereas the transformation of test pattern *r2* into 1-detection functional delay test will consider only PP faults {f, g}. Consequently, the functional delay faults that correspond to PP faults {b, c} will be detected using, for signal propagation, only one path. For example, let's analyze the circuit presented in Figure 1.
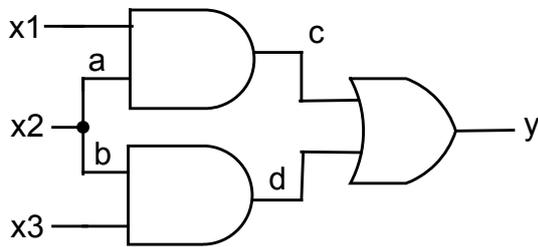

Figure 1. Example circuit

The test pattern set T1 (x1 x2 x3) = <110, 011, 010, 101> detects all functional PP faults. The transformation of test T1 according to approach [10] results into functional delay test T2 (x1 x2 x3) = <(010,110), (100, 110), (010,011), (110, 010), (011, 010), (111, 101)>. The functional delay fault coverage of test T2 is 100% alike. However, the application of test T1 and T2 shows different fault coverages at gate-level of circuit description. The test T1 detects all stuck-at faults whereas the test T2 doesn't detect the slow-to-rise transition fault on line *b*. The PP fault $(x1^0, y^0)$ is

detectable on two input patterns (x1 x2 x3) = <110>, (x1 x2 x3) = <011> and signal propagation from input *x2* to output *y* occurs through two different paths x2, a, c, y and x2, b, d, y. Therefore, the result is that the stuck-at faults a^0 and b^0 are detectable on the test T1. While the test T2 detects the corresponding functional delay fault (x2, y, r x2, r y) just once, using for signal propagation from input *x2* to output *y* the path x2, a, c, y. The outcome is that the slow-to-rise transition fault on line *b* is not detectable on the test T2.

The test generation is the most complex and most computer resources demanding activity in the design process of digital devices. Therefore, naturally there arises the implication that it is desirable by construction of functional delay test to utilize all information about static fault detection, which is available in the PP fault test. Suppose, we have 1-detection PP fault test T^{PP} of length L. Then the number of detections of particular PP fault may range from 1 to L. Thus, in the next section, we will use, for PP test transformation into functional delay test, the fault model proposed in [8] according to which Δ different test patterns per fault are generated. However, in our case the number of detections Δ will be different not only for various circuits but will vary for particular faults of the same circuit. Let's say that the test pattern test T^{PP} detects PP fault *q* times. Then the corresponding functional delay fault test T^{FD} will detect adequate functional delay fault *q* times too where $1 <= q <= L$.

4. Experimental results

The non-redundant ISCAS'85 benchmark circuits have been selected for experiments. The functional delay tests have been derived from PP fault tests according to approach presented in [10]. The test sets for PP faults were generated for the black-box model of the circuit [4] using a random search procedure. The black-box models were written in the C programming language.

Table 1. Transition fault detection by functional delay SIT tests

| Circuit	1-detection		n-detection			n-detection limited		
	Coverage (%)	Test size	Coverage (%)	Test size	n max	Coverage (%)	Test size	n limited SIT
C432	95.56	348	98.33	966	25	98.33	828	5
C499	94.40	5180	94.4	37053	570	94.4	5180	1
C880	98.91	1001	100	14261	166	100	12996	75
C1355	97.13	5162	97.13	34895	540	97.13	5162	1
C1908	95.24	2359	95.9	15925	333	95.9	12074	50
C2670	96.51	1820	99.72	27918	255	99.72	10342	11
C3540	83.08	1457	98.76	14516	216	98.76	9992	28
C5315	98.41	4950	99.9	106957	754	99.9	45003	25
C6288	99.75	1065	100	8576	75	100	7700	22
C7552	99.21	5801	99.95	184720	1263	99.95	153231	200
Average	95.82	2914	98.41	44579	420	98.41	26251	42

Table 2. Transition fault detection by functional delay MIT tests

Circuit	1-detection		n-detection			n-detection limited		
	Coverage (%)	Test size	Coverage (%)	Test size	n max	Coverage (%)	Test size	n limited MIT
C432	94.69	244	96.88	577	25	96.88	471	4
C499	93.00	1159	94.14	1437	570	94.14	1407	400
C880	100.00	743	100.00	4871	166	100.00	743	1
C1355	95.01	1068	96.81	1362	540	96.81	1342	450
C1908	94.58	1814	95.94	10830	333	95.94	10197	100
C2670	98.21	1117	99.66	9514	255	99.66	6612	40
C3540	94.21	1166	98.86	8820	216	98.86	7360	50
C5315	99.91	3382	99.97	32796	754	99.97	9506	7
C6288	99.89	903	100.00	5810	75	100.00	2674	7
C7552	98.03	4331	99.77	42412	1263	99.77	40026	250
Average	96.75	1593	98.20	11843	420	98.20	8034	131

The experimental results of transition fault detection by functional delay tests are presented in Tables 1 and 2. The obtained test quality is characterized by transition fault coverage and test size expressed as the number of test pattern pairs.

Let's analyze presented experimental results. The application of n-detection functional delay SIT tests allowed improving the transition fault coverage in comparison with 1-detection tests from 95.8% to 98.4% on the average. The average improvement is 2.6% whereas the best result is for circuit C3540 (15.7%) and the circuits C499 and C1355 show no improvement. However, the increment of test length is very high. The test length is, on the average, approximately 15 times higher than in the case of 1-detection tests. The application of n-detection functional delay MIT tests showed a little worse result. The average improvement of transition fault coverage was 1.45% whereas the best result is as well for circuit C3540 (4.65%) and the test quality increment was observed for all circuits but C880 for which the 1-detection MIT test already reached 100% transition fault coverage. The test length increased on the average 7 times. Comparing SIT and MIT tests, we see that 1-detection MIT tests possess higher quality than SIT tests because they are, on the average, almost two times shorter and their transition fault coverage is, on the average, 0.9% higher. On the other hand, the comparison of n-detection tests indicates that the transition fault coverage of SIT tests is, on the average, 0.2% higher than that of MIT tests.
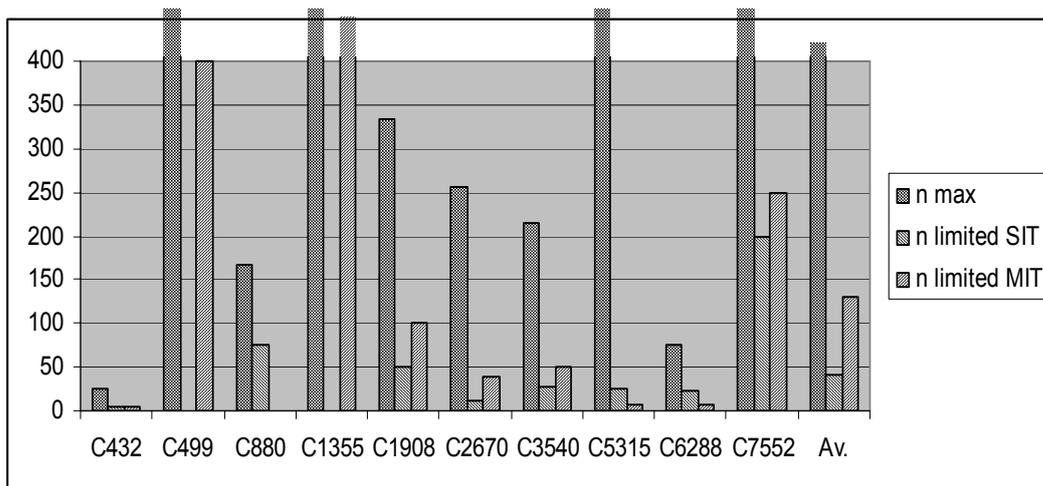
Figure 2. The numbers of fault detections

Another remark is that the maximum number of detections of particular fault is very high and reaches on the average 420 (see columns under heading "n max"). Such high number of the fault detections may occur only for faults for which the conditions of signal propagation from circuit input to output are very simple, for example, through one inverter. Our investtigations of structural level circuit descriptions approved this assumption. Thus there is no sense to detect the particular functional delay fault using the

maximum number of detections because the same path will be sensitized many times. Therefore, we made additional experiments which results are presented in the last three columns of Tables 1 and 2. The aim of these experiments was to find a minimal necessary number of detections (*n limited*) that warrants the same transition fault coverage as *n maximal*. The limitation of *n* allowed us to shorten the SIT test size almost twice and MIT test approximately 30% on the average. However, we couldn't find out one common for all circuits limit of fault detections or discover at least the relation between *n max* and *n limited* in order to restrict the number of fault detections for particular circuit. There is no correlation between these two variables (see the chart in Figure 2). Furthermore, the relationship between *n limited* for SIT test and *n limited* for MIT test doesn't exist too. Therefore, we propose by transformation of PP test into functional delay test to use the maximal number of fault detections for particular fault.

Next we provide some arguments that support our proposition. In general, the test generation task at the algorithmic level is more complicated than at the gate level because all possible realizations of design must be taken into account. Therefore, the tests are larger compared to tests for particular realization of the circuit. However, the test generation at algorithmic level can be done in parallel with the circuit synthesis process and then the suitable test patterns for the synthesized gate level implementation have to be selected on the base of the fault simulation. This possibility allows reducing the overall time of design process because either the stage of test design is not necessary at all or the time for this stage is quite short since the augmentation of test is required only for the undetected faults. In order to obtain tests for particular implementation we have developed a simple automated test pattern selection tool. The experimental results regarding test pattern selection are presented in Tables 3 and 4.

Table 3. Test pattern selection, SIT test

	SIT test						TetraAMAX
	1-detection		n-detection		n-detection limited		
Circuit	Test size	Test size selected	Test size	Test size selected	Test size	Test size selected	
C432	348	193	966	219	828	219	142
C499	5180	526	37053	577	5180	526	223
C880	1001	471	14261	534	12996	534	137
C1355	5162	516	34895	534	5162	516	287
C1908	2359	532	15925	586	12074	584	316
C2670	1820	808	27918	940	10342	940	259
C3540	1457	787	14516	1156	9992	1155	403
C5315	4950	1657	106957	1942	45003	1933	301
C6288	1065	595	8576	650	7700	650	122
C7552	5801	1268	184720	1449	153231	1452	461
Average	2914	735	44579	859	26251	851	265

Table 4. Test pattern selection, MIT test

	MIT test					
	1-detection		n-detection		n-detection limited	
Circuit	Test size	Test size selected	Test size	Test size selected	Test size	Test size selected
C432	244	101	577	114	471	114
C499	1159	259	1437	273	1407	273
C880	743	195	4871	219	743	195
C1355	1068	283	1362	318	1342	318
C1908	1808	306	10830	379	10197	378
C2670	1117	351	9514	415	6612	444
C3540	1166	477	8820	643	7360	639
C5315	3228	554	32796	640	9506	600
C6288	863	315	5810	394	2674	390
C7552	4331	691	42412	837	40026	836
Average	1573	353	11843	423	8034	419

If we analyze the test sizes presented in Tables 3 and 4, we see that the test length reduction in all cases is very high. It ranges from 4 to 52, i.e. the length of selected 1-detection SIT test is 4 times less than of initial test and 52 times less in case of n-detection SIT test. The obtained test sizes are comparable, especially of MIT tests, with sizes of tests generated using commercial Synopsys test pattern generator for transition faults TetraMAX (see last column of Table 3). However, it should be noted that TetraMAX for all circuits generated the tests that exposed 100% transition fault coverage. If we separately consider SIT and MIT tests, we can notice that the test sizes obtained after test pattern selection are very similar. But the selected MIT tests are on average 2 times shorter than the selected SIT tests. The last and essential observation of our investigations is that the test sizes of 1-detection, *n max* and *n limited* modes differ, after selection, very little (less than 20% on the average). The test size together with fault coverage is crucial parameter describing test quality of manufacturing test. However, the test length is not so important for tests that are designed for verification purposes. Therefore, we conclude that by transformation of PP test into functional delay test it is advisable to use the maximum number of detections of particular fault. Thus, the test engineer has to choose by employment of functional delay test for detection of structural transition faults between SIT test, which takes longer application time, however, consumes less power, and MIT test, which power consumption is higher yet which test application time is shorter.

5. Conclusions

The test generation is the most complex and most computer resources demanding activity in the design process of digital devices. Thus while constructing the functional delay test it is desirable to utilize all information about static fault detection which is available in the pin pair fault test. We suggest while transforming the pin pair test into functional delay test to use a variable number of fault detections. The experiments performed on ISCAS'85 benchmark circuits show the effectiveness of this proposal. The restriction of number of fault detections allowed us to shorten the test size almost twice. However, there is no one common for all circuits limit of fault detections and no relation between *n max* and *n limited* which could allow restricting the number of fault detections for particular circuit. Therefore, while transforming the pin pair test into functional delay test we propose to use the maximum number of detections of particular fault. The experiments performed with functional test adaptation for testing of structural level faults supported this approach.

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