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FUNCTIONAL DELAY TEST QUALITY ASSESSMENT AT HIGH LEVEL OF ABSTRACTION

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Abstract. The test can be developed at the functional level of the circuit. Such an approach allows developing the test at the early stages of the design process in parallel with other activities of this process. The main problem is the quality assessment of the functional test because the implementation of the circuit is not available yet. The paper presents the criteria of the quality assessment of the functional test consisting of the pairs of patterns with multiple signal transition. The introduced criteria are based solely on the primary input values and the primary output values of the programming prototype. The use of the indirect impact of the inputs to the outputs in the criteria of the quality assessment is introduced for the first time. The presented experimental results explore the relationship between the value of the presented criterion and the transition fault coverage at the gate level. The increased quality of the functional test means the higher transition fault coverage.

1. Introduction

The functional test is based on the function of the circuit, which can be designed in many ways. The possible defects of the circuit depend on the implementation. The test is usually developed according to the specific implementation and it is devoted to detect the defects of this particular implementation. The manufacturing test can be developed only on the base of the specific implementation. Meanwhile, the functional test is not related to the particular implementation. In such a case, the functional test should be able to detect the faults of all the possible implementations. Therefore, to develop the functional test is more complex problem than to develop the test for a particular implementation. The main problem, which we are facing during the development of the functional test, is the quality assessment of the functional test when the particular implementation is not available. The already known models of the functional faults enable to develop the functional test, which detects more than 99% of stuck-at faults of any implementation of the circuit function [0]. But such a functional test is several times longer than the test developed for the particular implementation of the circuit. The functional test must be minimized according to the particular implementation when it is used as the base for the manufacturing test. Furthermore, the functional test can be augmented according to undetected faults of the particular implementation. The main advantage of the functional test is that it can be developed at the early stages of the design according to the programming prototype in parallel with synthesis process. Meanwhile, the minimization of the functional test after synthesis according to the particular implementation doesn't require the long hours and it has a weak impact on the overall time of the design.

With ever shrinking geometries, growing density and increasing clock rate of chips, delay testing is gaining more and more industry attention to maintain test quality for speed-related failures. The purpose of a delay test is to verify that the circuit operates correctly at a desired clock speed. The pair of test patterns is used to detect delay faults. The first pattern sets the initial values on the inputs of the circuit; the second pattern launches the transition. The functional test can be used also to detect delay faults, when the test patterns are grouped in the pairs.

The field of functional test development for delay faults is not investigated quite enough. The possibilities of the detection of the delay faults for the particular implementation by the functional test are also unknown. Furthermore, the criteria of the quality assessment of the functional test according to the delay faults of the particular implementation are not investigated quite well. The criteria of the quality assessment of the functional test according to the stuck-at faults of the particular implementation that can be used to evaluate the detection of the delay faults do not suit quite well for such a purpose, because the detection of the delay faults requires the pair of test patterns. This paper investigates and presents some solutions for the aforementioned problems.

2. Related work

The testing engineer prepares the functional test according to the specification of the device. The functional test is used to verify the next steps of the design and it can be used for the development of the manufacturing test as well. Such a test usually verifies the function of the device and it cannot guarantee the full coverage of the stuck-at faults at the gate level of the device. Therefore, when the synthesis of the device is completed, the list of undetected faults is formed, and the deterministic methods are used to detect the faults from this list. Any functional test can be used to detect the delay faults. The pairs of test patterns are formed, when every test pattern, except the first one and the last one, is repeated two times. In this case, the pairs of test patterns are formed in the following way: the first and the second patterns, the second and the third patterns, and etc.

During design process the software prototype of the device is created according to the specification. The software prototype simulates the functions of the device, enables to calculate the output values according to the input values, and can be regarded as the black-box model of the device. The functional test can be generated on the base of the software prototype. Several black-box fault models were suggested that do not examine the description code but they are based on the input stimuli and the output responses [0]-[0]. The most prominent is the single coupling fault model proposed in [0] and extended in [0], which is defined in terms of a single input/output pair, considers the influence of the input value change to the output value change. The definition of coupling fault is realization-independent and combinational [0]. The set of all test vectors for a coupling fault is called coupling test set. The average size of the coupling test set is 2^n - 1, where n denotes the number of inputs of the module [0]. The only elementary n-input (gate) functions, i.e. AND, OR, NAND, and NOR require $n + 1$ coupling test. Therefore, the coupling test sets are very large even for small modules. The implementation of test generation program COTEGE for coupling faults limited the number of module inputs to at most 20; meanwhile, the XOR function was limited only to 6 inputs [0]. The presented results of efficient test generation using COTEGE cannot be attributed only to coupling fault model, because COTEGE was developed for combinational modular circuits whose functional behavior is specified hierarchically. COTEGE computed test sets for each module separately. Then the test set for the whole circuit was generated with respect to the inputs of circuit by using high-level techniques [0] based on PODEM [0], which has no relation to the coupling fault. After all coupling faults are detected, reverse-order fault simulation is performed for test compaction purposes, which also has no relation to the coupling fault.

The functional fault models [0] that are named pin pair (PP) and pin triplet (PT) enable to develop the functional test on a base of the software prototype at the early stages of the design process, while the synthesized description of the device is not available yet. The functional delay test developed on the base of test for PP faults detects on the average more than 95 per cent of the transition fault of ISCAS85 circuits [0]. The investigation of test development methods based on PP test showed that the coverage of transition faults could be increased on the average till 99 per cent [0]. On the base of these experiments the conclusion was made, that single input change is not enough to reach the full transition fault coverage. The multiple input change pairs of test patterns expand the possibilities of detection of transition faults by the functional test.

The functional test can be created on the base of behavioral level fault models that are related to the description code [0-0]. Various sophisticated test generation methods were developed that enable to reach the coverage of stuck-at faults at the gate level that varies in the range from 70 to 97 per cent [0]. The development of functional test for delay faults based on the synthesizable description code and its quality assessment at the functional level are not investigated quite well yet.

The object of this paper is the quality assessment of the functional delay test according to the software prototype of the device. The quality assessment is based on the primary input values and the primary output values.

The main purpose of the paper is to analyze and to propose the criteria of the quality assessment of the functional delay test at a high level of description when the implementation details are not available yet that the generated test would detect the delay faults of any possible implementation. Then, such a test can be adjusted to the gate level of particular implementation by means of fault simulation in order to delete the test patterns, which do not detect the new faults and the resulting test can be used as the manufacturing test. This possibility allows reducing the overall time of design process, because either the stage of test design is not necessary at all or the time for this stage is quite short when the augmentation of test is required only for the undetected faults.

This paper presents the criteria for the quality assessment of the functional delay test at a high level of description for the first time. The main difference from the criteria, which are used for PP fault model, is that the pairs of test patterns can have multiple changes on the inputs. Meanwhile, PP fault model is based on the single input value change. The test generation based on PP fault model examines the impact of the input value change to the output value change. The idea of this paper is that the quality assessment of the functional delay test can be based on the establishment of the relationship between the disabled input value change and the disappearance of the value change on the outputs. Such an approach allows assessing all possible pairs of patterns of the functional delay test. The new possibility, which allows

assessing the indirect impact of the input value change to the output value change, was discovered.

3. The criteria to assess the quality of the functional test

Two test patterns are needed in order to detect the delay faults. Some values on the inputs of test patterns pair are different that mean the change of the value, and some values are constant. The changes can be either single or multiple. Only the value change on the inputs that invokes the value change on the outputs can detect the delay faults. The value changes from the inputs are propagated to the outputs along the paths of the circuit. The usual way to detect the delay faults is to propagate the signal transition along the several longest paths of the circuit. In order to assess the quality of the functional test it is necessary to determine which input signal transition influences the particular output signal transition. It is not an easy task when the signal transitions are observed on the multiple inputs. Therefore, it is expedient to examine the influence of the blocking of separate input signal transitions to the output signal transitions. The signal transitions on the inputs will be blocked one by one keeping the value in the second pattern the same as the value in the first one.

An example will be used to explain in details the concept of the blocking of the input signal transition. Let's say, there exists the pair of input patterns {1010, 0111}, where the signal transitions are observed on the first, the second, and the fourth inputs. When the transition is blocked on the first input, the pair of patterns becomes the following: {1010, 1111}. When the transition is blocked on the second input, the pair of patterns becomes the following: {1010, 0011}. When the transition is blocked on the fourth input, the pair of patterns becomes the following: {1010, 0110}. The transition blocking on the input may disable the transitions on some outputs. If such a case is observed it means that the blocked transition on the input influences the transition on the output where the transition was disabled. The following four cases have to be considered:

1. The blocked transition 0→1 on the input disables the transition 0→1 on the output;
2. The blocked transition 0→1 on the input disables the transition 1→0 on the output;
3. The blocked transition 1→0 on the input disables the transition 0→1 on the output;
4. The blocked transition 1→0 on the input disables the transition 1→0 on the output.

The blocked transition on the input directly influences the disappearance of the transition on the output. Therefore, such a relationship will be called direct impact, which corresponds to the robust detection of the delay faults. The indirect impact is possible also when the blocked transition on the input invokes the transition on the output that had no transition before. Such a relationship shows that the considered transition on the input blocked the influence of the transition on some other input, and, when this transition was disabled, the additional transition appeared on the output, on which it was not observed. The following four cases can be considered as well:

1. The blocked transition 0→1 on the input invokes the additional transition 0→1 on some output;
2. The blocked transition 0→1 on the input invokes the additional transition 1→0 on some output;
3. The blocked transition 1→0 on the input invokes the additional transition 0→1 on some output;
4. The blocked transition 1→0 on the input invokes the additional transition 1→0 on some output.

The indirect impact corresponds to the non-robust detection of the delay faults.

In general, let's say, there exist two input patterns: $P^1 = <p_1^1, p_2^1, \ldots, p_i^1, \ldots, p_n^1>$, and $P^2 = <p_1^2, p_2^2, \ldots, p_i^2, \ldots, p_n^2>$ where n is the number of inputs, and their responses: $R^1 = <r_1^1, r_2^1, \ldots, r_j^1, \ldots, r_m^1>$, and $R^2 = <r_1^2, r_2^2, \ldots, r_j^2, \ldots, r_m^2>$, where m is the number of outputs. The impact of the signal transitions on the inputs to the signal transitions on the outputs can be represented by the impact matrix $\|X\|_{2nx4m}$. The input i is represented by two rows: $2i$-1, and $2i$ in the matrix. The row $2i$-1 corresponds to the signal transition 0→1 on the input, and the row $2i$ corresponds to the signal transition 1→0 on the input. The output j is represented by four columns. The column $4j$-3 stands for the direct impact of signal transition on the input to the signal transition 0→1 on the output. The column $4j$-2 stands for the direct impact of signal transition on the input to the signal transition 1→0 on the output. The column $4j$-1 stands for the indirect impact of signal transition on the input to the signal transition 0→1 on the output. The column $4j$ stands for the indirect impact of signal transition on the input to the signal transition 1→0 on the output.

The entry of matrix X is set to 1 if the disabled signal transition on the input disables or invokes the signal transition on the output:

- The entry $x_{2i-1,4j-3}=1$ if $p_i^1=0$, $p_i^2=1$, $r_j^1=0$, $r_j^2=1$, and after setting $p_i^2=0$, the response is $r_j^2=0$;
- The entry $x_{2i-1,4j-2}=1$ if $p_i^1=0$, $p_i^2=1$, $r_j^1=1$, $r_j^2=0$, and after setting $p_i^2=0$, the response is $r_j^2=1$;
- The entry $x_{2i-1,4j-1}=1$ if $p_i^1=0$, $p_i^2=1$, $r_j^1=0$, $r_j^2=0$, and after setting $p_i^2=0$, the response is $r_j^2=1$;
- The entry $x_{2i-1,4j}=1$ if $p_i^1=0$, $p_i^2=1$, $r_j^1=1$, $r_j^2=1$, and after setting $p_i^2=0$, the response is $r_j^2=0$;
- The entry $x_{2i,4j-3}=1$ if $p_i^1=1$, $p_i^2=0$, $r_j^1=0$, $r_j^2=1$, and after setting $p_i^2=1$, the response is $r_j^2=0$;
- The entry $x_{2i,4j-2}=1$ if $p_i^1=1$, $p_i^2=0$, $r_j^1=1$, $r_j^2=0$, and after setting $p_i^2=1$, the response is $r_j^2=1$;
- The entry $x_{2i,4j-1}=1$ if $p_i^1=1$, $p_i^2=0$, $r_j^1=0$, $r_j^2=0$, and after setting $p_i^2=1$, the response is $r_j^2=1$;

- The entry $x_{2i,4j}=1$ if $p_i^1=1$, $p_i^2=0$, $r_j^1=1$, $r_j^2=1$, and after setting $p_i^2=1$, the response is $r_j^2=0$.

Let's consider the 2-inputs AND gate. The pair of patterns $P^1=<0, 0>$, $P^2=<1, 1>$ are fed to the inputs, and the responses are as follows: $R^1=<0>$, $R^2=<1>$. The signal transitions are on both inputs and on the output: $p_1(0\rightarrow1)$, $p_2(0\rightarrow1)$, $r_1(0\rightarrow1)$. The impact of the signal transitions on the inputs to the signal transitions on the outputs will be represented by the matrix $||X||_{4x4}$. The blocking of the signal transition on the first input $p_1(0\rightarrow0)$ disables the signal transition on the output $r_1(0\rightarrow0)$, and the entry $x_{1,1}$ will be set to 1. Similarly, the blocking of the signal transition on the second input $p_2(0\rightarrow0)$ disables the signal transition on the output $r_1(0\rightarrow0)$, and the entry $x_{3,1}$ will be set to 1. For the pair of patterns $P^1=<1, 1>$, $P^2=<0, 1>$ and responses $R^1=<1>$, $R^2=<0>$, the entry $x_{2,2}$ will be set to 1. For the pair of patterns $P^1=<1, 1>$, $P^2=<1, 0>$ and responses $R^1=<1>$, $R^2=<0>$, the entry $x_{4,2}$ will be set to 1. For the pair of patterns $P^1=<1, 1>$, $P^2=<0, 0>$ and responses $R^1=<1>$, $R^2=<0>$, no one entry will be set to 1, because the blocking of the signal transition on the input does not disable the signal transition on the output. The pair of patterns $P^1=<0, 1>$, $P^2=<1, 0>$ as well as the pair of patterns $P^1=<1, 0>$, $P^2=<0, 1>$ both have the same responses without signal transition $R^1=<0>$, $R^2=<0>$. But the blocking of the signal transition on the input ($p_2(1\rightarrow1)$ or $p_1(1\rightarrow1)$) invokes the signal transition on the output $r_1(0\rightarrow1)$. Such a result means the indirect impact of the signal transition on input to the signal transition on the output, and the entries $x_{4,3}$ and $x_{2,3}$ will be set to 1. The results for all the possible pairs of patterns are presented 0. The unnumbered rows of 0 show the blocked signal transitions on the inputs that disable or invoke the signal transition on the output, and, therefore, the appropriate entry of the matrix X is set to 1. As we can see, the blocking of the signal transition on the inputs in the pairs of patterns presented in the rows numbered 1, 2, 4, 7, 10 has no influence on the response on the output. The pair of patterns presented in the row No.3 determines the same impact as the pairs of patterns presented in rows No.6 and No.9 together. The matrix X is presented in 0.

Table 1. Analysis of the pairs of patterns

No.	The pair of patterns	p_1	p_2	r_1	X
1	$P^1=<0,0>$, $P^2=<0,1>$,$R^1=<0>$, $R^2=<0>$	0→0	0→1	0→0	
2	$P^1=<0,0>$, $P^2=<1,0>$,$R^1=<0>$, $R^2=<0>$	0→1	0→0	0→0	
3	$P^1=<0,0>$, $P^2=<1,1>$,$R^1=<0>$, $R^2=<1>$	0→1	0→1	0→1	
		0→0	0→1	0→0	$x_{1,1}=1$
		0→1	0→0	0→0	$x_{3,1}=1$
4	$P^1=<0,1>$, $P^2=<0,0>$,$R^1=<0>$, $R^2=<0>$	0→0	1→0	0→0	
5	$P^1=<0,1>$, $P^2=<1,0>$,$R^1=<0>$, $R^2=<0>$	0→1	1→0	0→0	
		0→1	1→1	0→1	$x_{4,3}=1$
6	$P^1=<0,1>$, $P^2=<1,1>$,$R^1=<0>$, $R^2=<1>$	0→1	1→1	0→1	
		0→0	1→1	0→0	$x_{1,1}=1$
7	$P^1=<1,0>$, $P^2=<0,0>$,$R^1=<0>$, $R^2=<0>$	1→0	0→0	0→0	
8	$P^1=<1,0>$, $P^2=<0,1>$,$R^1=<0>$, $R^2=<0>$	1→0	0→1	0→0	
		1→1	0→1	0→1	$x_{2,3}=1$
9	$P^1=<1,0>$, $P^2=<1,1>$,$R^1=<0>$, $R^2=<1>$	1→1	0→1	0→1	
		1→1	0→0	0→0	$x_{3,1}=1$
10	$P^1=<1,1>$, $P^2=<0,0>$,$R^1=<1>$, $R^2=<0>$	1→0	1→0	1→0	
11	$P^1=<1,1>$, $P^2=<0,1>$,$R^1=<1>$, $R^2=<0>$	1→0	1→1	1→0	
		1→1	1→1	1→1	$x_{2,2}=1$
12	$P^1=<1,1>$, $P^2=<1,0>$,$R^1=<1>$, $R^2=<0>$	1→1	1→0	1→0	
		1→1	1→1	1→1	$x_{4,2}=1$

Now we present the algorithm that fills up the matrix $||X||_{2n\ x\ 4m}$ according to the input patterns and their responses on the outputs (0). Initially, the matrix X is filled up with zeros. The responses are calculated for the pair of input patterns (line 2). The loop is repeated for every primary input of the circuit. The value of the input is complemented and assigned to the variable *d* (line 3). The interest is only for the pair of values which differ. The signal transition is blocked, and the response is calculated (line 4). Next, all the values on the outputs are checked. The interest is only for the values which indicate the difference between the fault-free and the faulty pattern. The control statement in the line 7 indicates what impact

is: direct (line 7) or indirect (line 8). The use of the variables *d* and *c* allows writing indices for the matrix entries in the compact form.

Table 2. Impact matrix X

Inputs	Output			
	Direct impact		Indirect impact	
The first input	1	0	0	0
	0	1	1	0
The second input	1	0	0	0
	0	1	1	0

1. $X=||x_{i,j}:=0||_{2nx4m}$;
2. $R^1:=f(P^1)$; $R^2:=f(P^2)$;
3. DO i: =1,2,3,...,n; P^3: $=P^2$; d:=1- p^1_i;
4. IF ($p^1_i \neq p^2_i$) THEN $p^3_i:=1- p^2_i$; $R^3=f(P^3)$;
5. DO j: =1,2,3,...,m; c:=3- r^1_j;
6. IF ($r^3_j \neq r^2_j$) THEN
7. IF($r^2_j \neq r^1_j$) THEN $x_{2i-d,4j-c}:=1$;
8. ELSE $x_{2i-d,4j-c+2}:=1$;
9. ENDIF;
10. ENDIF;
11. ENDDO;
12. ENDIF;
13. ENDDO;

Figure 1. The algorithm that fills up the impact matrix

The new criterion *K* for the quality assessment of the functional delay test is introduced. The criterion *K* is based on the matrix *X* and is calculated as follows:

$$K = k_1 \sum_{j=1}^{m} \sum_{i=1}^{2n} (x_{i,4j-3}+x_{i,4j-2}) + k_2 \sum_{j=1}^{m} \sum_{i=1}^{2n} (x_{i,4j-1}+x_{i,4j}) \quad (1)$$

The sum of the values, which represent the direct impact, is multiplied by the coefficient k_1, and the sum of the values, which represent the indirect impact is multiplied by the coefficient k_2. The values of the factors k_1 and k_2 allow to have different criteria. When k_2=0, then only the direct impact will be considered, and, in the opposite, when k_1=0, then only the indirect impact will be considered. The appropriate values of the coefficients can be selected during the experiments in order to have the direct relationship between the quality assessment of delay faults at the functional level and the quality assessment of delay faults at the gate level. The values of the coefficients can be adapted to the different classes of the circuits as well.

Two different pairs of input patterns, which determine the same impact between the input values and the output values, are not equivalent, because they can even for the same implementation of the circuit sensitize the different paths of the circuit and they can detect the different delay faults. Therefore, it is expedient for the quality assessment of the functional test to count the number of pattern pairs that allow the input to influence the appropriate output. The entries of the matrix *X* may hold such a number. Such a matrix will be denoted as X^{Δ}. In such a way, the longer test will have the bigger value of the quality assessment. Therefore, it is meaningful to use the limit Δ, which would indicate how many times the input value influences the output value. The different Δ values would indicate the different criteria of quality assessment of the functional test. The size of the test also depends on the value Δ. When Δ is big, the size of the test can become unacceptable. The choice of the limit Δ has to be based on the compromise between the size of the test and the coverage of the delay faults at the gate level. It needs to pay an attention to the important drawback of such an approach. If the same test would be repeated twice, the value *K* would become twice greater, but the coverage of the delay faults at the gate level would remain the same. Therefore, the increase of the value Δ has only the meaning, when the functional test has no the same pairs of test patterns. Another possible important drawback of the limit Δ is that the values of the test patterns may differ on such inputs that the impact of the input to the output will be propagated by the same path, and the new delay faults will not be detected at the gate level. The latter drawback has no simple remedy.

The formula (1) can be generalized on the base of the limit Δ. The formula (1) corresponds to the case where the limit Δ that is equal to 1. When Δ>1, the lines 7, 8 and 9 in 0 have to be changed as follows:

7. IF($r^2_j \neq r^1_j$) THEN IF $x_{2i-d,4j-c}<\Delta$ THEN $x_{2i-d,4j-c}:= x_{2i-d,4j-c}+1$;
   ENDIF;
8. ELSE IF $x_{2i-d,4j-c+2}<\Delta$ THEN $x_{2i-d,4j-c+2}:= x_{2i-d,4j-c+2}+1$;
   ENDIF;
9. ENDIF;

In the general case, the criterion K^{Δ} for the matrix X^{Δ} takes the following form:

$$K^{\Delta} = k_1 \sum_{j=1}^{m} \sum_{i=1}^{2n} (x^{\Delta}_{i,4j-3}+x^{\Delta}_{i,4j-2}) + k_2 \sum_{j=1}^{m} \sum_{i=1}^{2n} (x^{\Delta}_{i,4j-1}+x^{\Delta}_{i,4j}) \quad (2)$$

It has to be noticed that some entries of the matrix are always zeros, because some inputs have no electric connections to some outputs. Such a situation makes the right quality assessment of the functional test more difficult, but it does not hinder to compare the quality of two functional tests of the same circuit.

Many paths usually exist between the inputs and the outputs. The use of limit Δ may not allow

propagating the impact of the input value to the output value along all possible paths. Therefore, the selected functional test cannot guaranty the full delay fault coverage at the gate level. We will investigate the relation between the quality assessment of the functional test and the transition fault coverage at the gate level in the next section.

4. The analysis of the proposed criteria of the quality assessment of the functional test

Firstly, we will investigate the coverage of functional delay test at the gate level, when Δ=1. The direct impact of the input value to the output value indicates that a pair of patterns activates the single-path or multi-path from the input to the output. If the single-path is activated, all the transition faults on this path are detected. Many single-paths can exist between the input and the output. That depends on the circuit implementation. The pair of patterns detects all the transition faults of the active single-path only. Such a path always exists if the input value influences the output value. But the opposite is not always true – a path between the input and the output does not exist if the input value has no influence on the output value. But it is possible to claim, if the path between the input and the output does not exist, the input value can not have the direct impact to the output value. The single-path is depicted in 0, where each square denotes a gate; the continuous line denotes the connections between gates; the dashed line denotes the multiple gates and their connections.

The multi-path is depicted in 0.

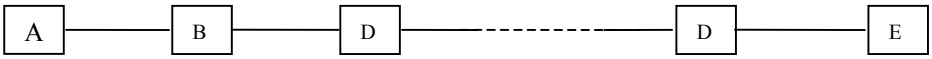

Figure 2. The single-path between gates *A* and *E*

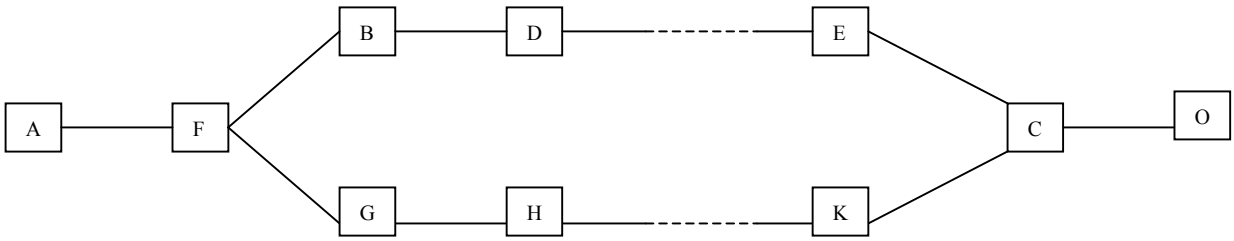

Figure 3. The multi-path between gates *A* and *O*

When the multi-path is activated (0), then the pair of patterns detects all the transition faults of the multi-path till the fan-out gate *F*, because this segment of the multi-path is a single-path. The detection of the transition faults on the branches of the multi-path depends on the function of fan-in gate *C*. Let's consider the possible cases on the example in 0. Let's say, the signal transition on the input of the multi-path (gate *A*) invokes the signal transitions on the both branches of the multi-path, and these signal transitions propagate to the inputs of fan-in gate *C*. Depending on the number of complemented signal values, the four cases of signal transitions are possible:

1. $p_1(1\rightarrow0)$, $p_2(1\rightarrow0)$;
2. $p_1(0\rightarrow1)$, $p_2(0\rightarrow1)$;
3. $p_1(1\rightarrow0)$, $p_2(0\rightarrow1)$;
4. $p_1(0\rightarrow1)$, $p_2(1\rightarrow0)$.

If the fan-in gate *C* is AND gate, in the case No. 1, the transition faults in the branches of the multi-path are not detected, but the transition faults in the segment from fan-in gate C to the primary output are detected. In the case No. 2, the transition faults are detected in the branches of the multi-path, and they are detected in the segment from fan-in gate *C* to the primary output, as well. In the cases No. 3 and No. 4, the transition faults are detected in the branch that has the signal transition (1→0) on the input of fan-in gate *C*. But, in these two cases, the signal transition from fan-in gate *C* does not propagate to the primary output, and transition faults in this segment are not detected. The signal transition does not exist on the primary output, therefore, the disabled signal transition on the input can not disable the signal transition on the primary output, and the impact of the signal transition on the input is not determined to the signal transition on the output, nevertheless, the transition faults are detected on the appropriate branch of the multi-path.

The symmetric situation appears when the fan-in gate is OR gate. The first and the second cases change their places. In cases No. 3 and No. 4, the transition faults are detected in the branch that has the signal transition (0→1) on the input of fan-in gate *C*. In the general case, any branch of the multi-path can have fan-ins and fan-outs. Therefore, the transition faults that are detected may not form a continuous path. The only transition faults that are detected in a single-path form a continuous path. In the case of the multi-path, the transition faults are detected only in some segments of this multi-path. In some cases, these segments may form continuous path from the primary input to the primary output.

The indirect impact of the input on the output indicates that the value on the output is influenced by the values on several inputs and the signal transition on the investigated input blocks the signal transition on the other input. Therefore, when the signal transition is disabled on the investigated input, the signal transition appears on the primary output. In such a case, the pair of patterns that determines the indirect impact does not activate the continuous path from the primary input to the primary output. Additionally, the transition faults are not detected in the segment from the fan-in gate to the primary output. Such a situation is depicted in 0.

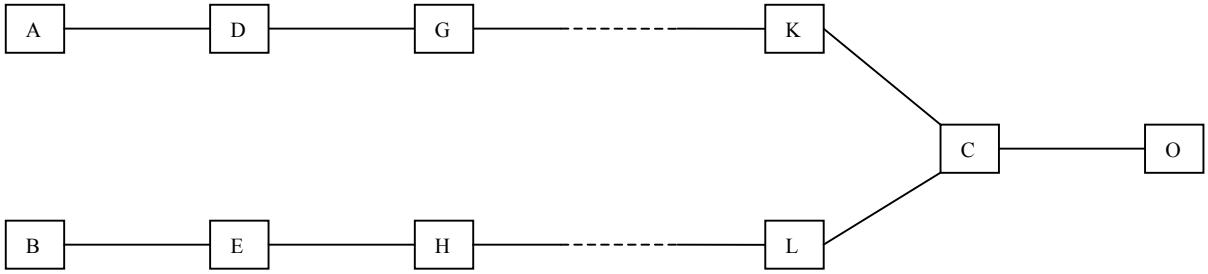

Figure 4. The multi-path that connects gates *A* and *C*, *B* and *C*

Let's say, the signal transition (0→1) propagates from the primary input *A* to the input of the fan-in gate *C*, which is AND gate, and the signal transition (1→0) propagates from the primary input *B* to the other input of the fan-in gate *C*. In such a case, there is no signal transition on the primary output. If the signal transition is disabled on the input *B*, the signal transition will appear on the primary output, because the signal transition from the input *A* propagates to the primary output. It means that the transition faults in the segment from the input *B* to the fan-in gate *C* are detected in non-robust way. Therefore, such an impact of the input on the output is called indirect. In this case, the transition faults are detected in the segment, which starts at the input with disabled signal transition and ends at the input of the fan-in gate. In the general case, it is possible to conclude that the determination of the direct impact of the input on the output allows detecting more faults than in the case of indirect impact, because the detected transition faults may form the continuous path. Additionally, the off-path transition faults that have relation to the path are detected as well. Meanwhile, the determination of the indirect impact always is related to the transition faults that lay only in the segment of the multi-path. Of course, it is possible to think of the contradictory example, but it is not the general case. These two assumptions will be the basis for choosing the values of the coefficients k_1 and k_2. The determination of the indirect impact increases the size of the functional delay test, because the additional test patterns related to the indirect impact are included into the test set. Therefore, the compromise has to be found between the size of test and the value of the quality criterion.

On the presumptions made before, we base the following conclusions on the quality assessment of the functional test. The quality of the functional test, when coefficient is $\Delta=1$, is determined by the sum of the entries of the matrix *X*. If such a criterion is not enough, then the value of the criterion of the quality assessment of the functional test can be corrected on the base of coefficient Δ specifically for the classes of circuits, and looking for the compromise between the size of the test and the coverage of the delay faults at the gate level of the circuit. The value of the coefficient Δ has to be chosen on the base of the experiments. During the experiments, it has to be determined:

- what size of the functional test statistically fits the chosen criteria of the quality assessment of the functional test?
- how many delay faults statistically are detected by the test patterns included as having the direct impact of the input to the output?
- how many delay faults statistically are detected by the test patterns included as having the indirect impact of the input to the output?
- how many delay faults statistically are detected by the test patterns included as having the direct and indirect impact of the input to the output?

For all the cases mentioned above, the influence of the value of the coefficient Δ on the test size and the coverage of delay faults has to be determined.

As we have noticed, the sum of the entries of the matrix X indicates the quality of the functional test. To obtain the maximal value K_{max} for the functional test, when coefficient $\Delta=1$, according to the programming prototype is quite a complex task, because not all the inputs have influence to the outputs, and the impact may propagate trough the even and/or uneven number of the inversions. The determination of the maximal value K_{max} of the non-zero entries is complicated in any case, even when the structure of the circuit is known, because the impact of the input can not be propagated along all the paths that connect the input and the outputs. K_{max} for the functional test can be obtained only analytically. These values are known for ISCAS85 benchmarks when coefficient $\Delta=1$ and $k_2=0$ [0]. The parameters of the circuits are presented in 0. As we can see, there is no direct relationship between K_{max} and the number of transition faults: For some

circuits, K_{max} exceeds the number of transition faults. For other circuits, K_{max} is lower than the number of transition faults.

Table 3. The parameters of the non-redundant ISCAS'85 benchmark circuits

Circuit	Gates	Inputs n	Outputs m	K_{max}, k_2=0	No of faults
C432	160	36	7	540	1412
C499	202	41	32	5184	3430
C880	383	60	26	1326	2396
C1355	546	41	32	5184	3350
C1908	880	33	25	3004	4848
C2670	1193	157	64	3320	5646
C3540	1669	50	22	2588	8960
C5315	2307	178	123	10540	13816
C6288	2406	32	32	3068	14422
C7552	3512	206	107	12188	19160

The relationship between the quality assessment of the functional test and the transition fault coverage has to be determined. The direct impact of the inputs on the outputs, when the patterns of the pair differ only by the single value, was investigated in [0]. The experiment has shown that the functional delay test (K_{max} was obtained, Δ=1, and k_2=0) detects on the average more than 95 per cent of transition faults at the gate level of the circuit.

The value of the criterion of the quality assessment of the functional test is not directly related to the number of detected transition faults, nevertheless, the general tendency exists that the increase of the value of the criterion means the higher number of detected transition faults. But it is not possible to state such a tendency when the pair of patterns has multiple signal transitions and the indirect impact will be evaluated. The additional investigation is required. But the quality assessment of the test that is generated at the gate level and that detects all the transition faults does not reach the maximal value of the criterion [0] (0, the second column). Such a result can be explained by the method of test generation that does not target to generate the test patterns for the sensitization all the paths between the inputs and the outputs. The path is sensitized only from the target fault to the output of the circuit. Meanwhile, the functional delay test targets to propagate the effects of transition faults along all the paths of the circuit. Such an objective allows propagating the effects of transition faults by longer paths.

The functional delay test of the maximal value K_{max} can detect the different number of the transition faults (0, third and fourth columns). The experiment reveals that the increased quality of the functional test means the higher transition fault coverage. When the coefficient Δ=2 ($K^{\Delta=2}_{max}$), the functional delay test detects more than 1 per cent of the transition faults (0, fifth column). When the coefficient Δ=4 ($K^{\Delta=2}_{max}$), the functional delay test detects the extra transition faults (0, sixth column) in comparison with the coefficient Δ=2.

Table 4. Influence of K_{max} to the transition fault coverage

Circuit	K/K_{max} %	Cov. (%) K^1_{max}	Cov. (%) K^2_{max}	Cov. (%) $K^{\Delta=2}_{max}$	Cov. (%) $K^{\Delta=4}_{max}$
C432	94.44	95.56	93.53	98.11	99.42
C499	74.71	94.40	94.40	94.40	94.40
C880	76.77	98.91	98.71	99.17	99.29
C1355	74.17	97.13	97.13	97.13	97.13
C1908	57.45	95.24	93.40	95.61	97.85
C2670	74.90	96.51	94.79	98.35	99.11
C3540	90.72	83.08	84.30	89.03	93.79
C5315	78.08	98.41	98.23	99.55	99.86
C6288	93.61	99.75	99.54	99.88	99.99
C7552	59.03	99.21	98.82	99.52	99.74
Aver.	77.38	95.82	95.29	97.08	98.06

5. Conclusion

The functional test can be developed in parallel with the other stages of the design and that does not increase the time-to-market. The quality of the functional test can be assessed in the initial stages of the design according to the programming prototype of the device. The suggested criteria of the quality assessment of the functional test are based solely on the primary input values and the primary output values. The increased quality of the functional test according to the suggested criteria means the higher transition fault coverage. The introduced criteria of the quality assessment of the functional test can be flexibly adapted for specific classes of the circuits in order to obtain the closer correlation between the value of the quality assessment of the functional test and the transition fault coverage at the gate level.

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